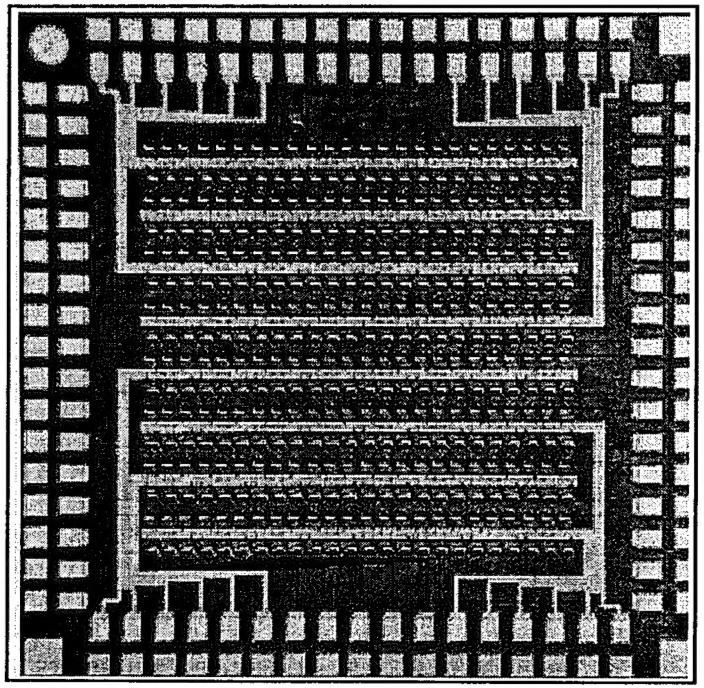
Final Report

Superconducting Infra Red Digital Processing (SIRDP)

10 K NbN Technology

Phase 1: NbN Foundry Maturity Assessment & Circuit Yield Quantification

Contract No. N00014-92-C-2130
TRW SN: 60044.000



For NRL/BMDO/M&S

December 1995

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Report Roadmap

Executive Overview

This project is the first to quantify a 10 K NbN process for uniformity and consistency and circuit yield. It is also the first step along a path of insertion of 10 K NbN technology into space systems. This section summarizes the achievements and projections of the NbN 10K technology

The Process

Process descriptions and trend data quantify the maturity and capability of the Class 10 NbN foundry. We improved TRW's NbN circuit fabrication capability from single gate yields to yielding 400 gates in around 18 months. Trend charts provide an estimate of attaining 1,000 gate circuits with acceptable yields.

The Logic Cell

A logic cell building unit was established and refined, resulting in larger operating margins, hence higher circuit performance yield.

The Results

The success of the program is attributed to the excellent, controlled foundry process, rigid, automated process control monitoring and testing. A large quantity of laboratory test data provided statistical significance to the observed results.

Report Content

Per MARTY NISENOFF
NRL / Code 6850
5/31/96

Executive Overview

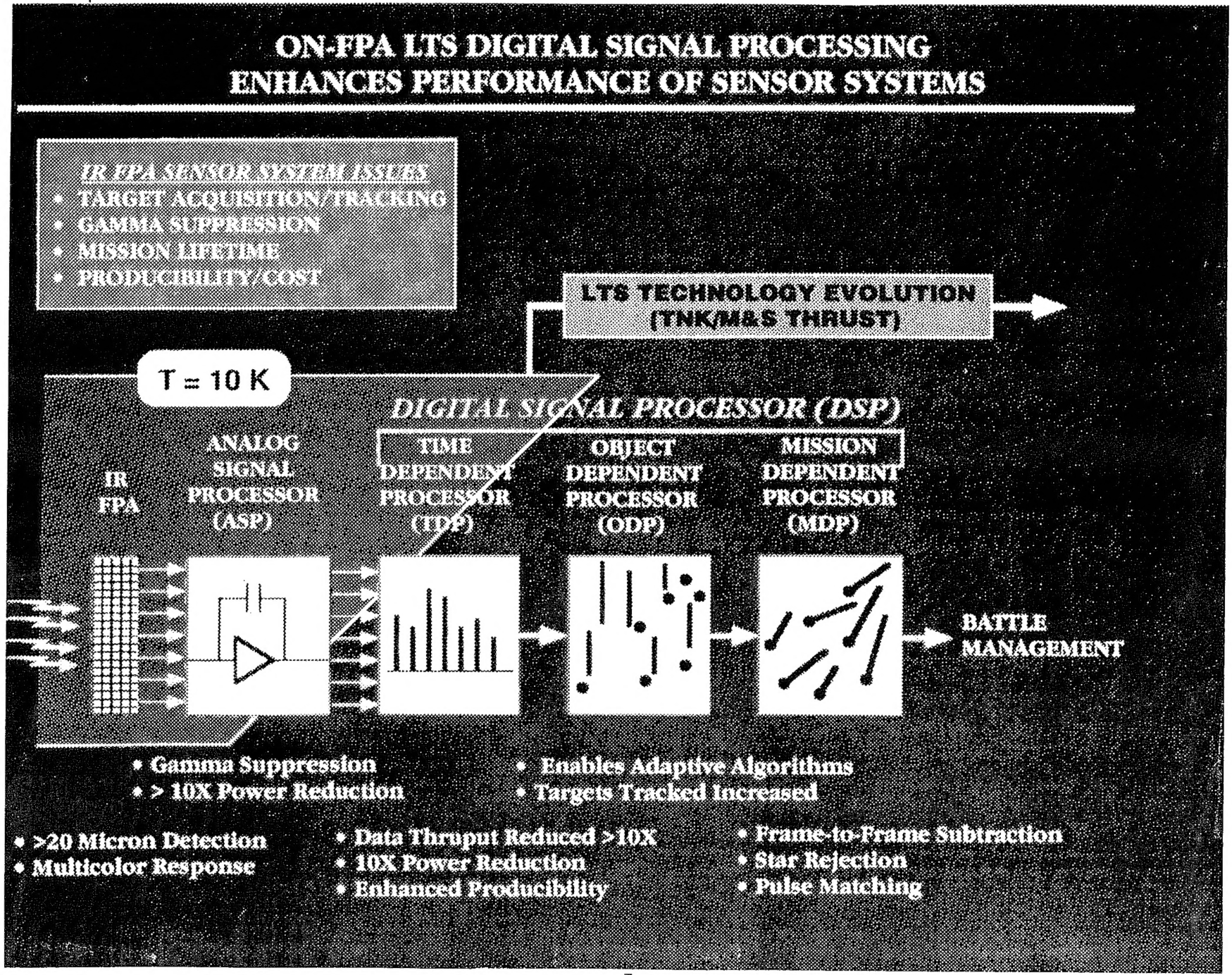
This project is the first to quantify a 10 K NbN process for uniformity and consistency and circuit yield. It is also the first step along a path of insertion of 10 K NbN technology into space systems. This section summarizes the achievements and projections of the NbN 10K technology

Executive Overview

The Interceptor Technology Directorate of Ballistic Missile Defense Organization (BMDO), is interested in exploring the impact of superconducting electronics technology on Infrared Focal Plane Array (FPA) Sensor Systems.

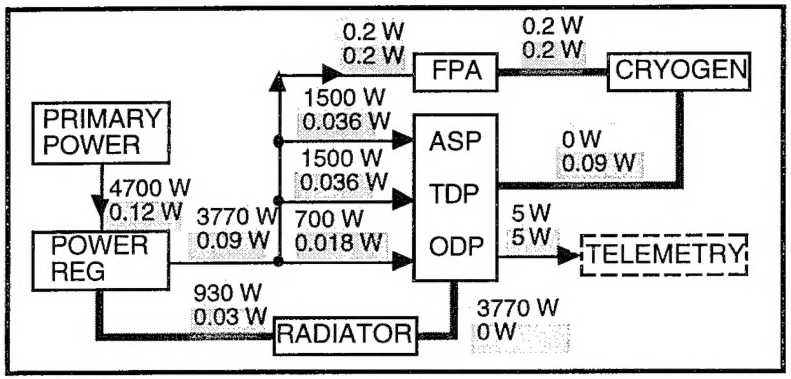
The thrust of this program is to assess the feasibility of using low temperature (~10 K) superconducting electronic technology to perform some of the functions done in the Time Dependent Processor (TDP) and Object Dependent Processor (ODP) (currently operating at ambient temperatures) of a cryogenically cooled focal plane assembly. The placement of superconducting TDP and ODP functions on the focal plane is enabled by the very low power dissipation of superconducting electronics. Movement of a significant number of these TDP and ODP functions onto the focal plane would provide many systems advantages, e.g.:

- Preprocessed digital signals reduce the signal-to-noise degradation crossing the large thermal gradient between cryogenic focal plane and ambient electronics.
- Digital signals on the cryogenic focal plane can be multiplexed more efficiently than analog signals, reducing the number of Input/Output (I/O) leads penetrating the cryogenic package, improving manufacturability and reducing thermal loading.
- High speed superconducting electronics on the focal plane permit systems designers to treat functions in a different fashion and could result in more efficient processing of, e.g., gamma suppression.
- Reduce total power and weight for comparable electrical performance and functionality


ON-FPA LTS DIGITAL SIGNAL PROCESSING
ENHANCES PERFORMANCE OF SENSOR SYSTEMS
IR FPA SENSOR SYSTEM ISSUES
• TARGET ACQUISITION/TRACKING
• GAMMA SUPPRESSION
• MISSION LIFETIME
• PRODUCIBILITY/COST
LTS TECHNOLOGY EVOLUTION
(TNK/M&S THRUST)
T = 10 K
DIGITAL SIGNAL PROCESSOR (DSP)
IR FPA
ANALOG SIGNAL PROCESSOR (ASP)
TIME DEPENDENT PROCESSOR (TDP)
OBJECT DEPENDENT PROCESSOR (ODP)
MISSION DEPENDENT PROCESSOR (MDP)
BATTLE MANAGEMENT
• Gamma Suppression
• > 10X Power Reduction
• Enables Adaptive Algorithms
• Targets Tracked Increased
• >20 Micron Detection
• Multicolor Response
• Data Thruput Reduced >10X
• 10X Power Reduction
• Enhanced Producibility
• Frame-to-Frame Subtraction
• Star Rejection
• Pulse Matching

This project was motivated by a systems study completed under an earlier BMDO project (Contract No. SDIO 84-88-C-0041). The impact of insertion of superconductive NbN based electronics technology operating at 10 K, on the weight, power, and performance of an IR FPA sensor was evaluated. This evaluation took into account the ripple through effect of processor improvements on such system characteristics as solar panel and thermal radiator weight, system and cryocooler power changes, and reduced package weight due to more compact processor packaging. By replacing large, heavy, high power boxes with small monolithic assemblies of superconducting chips, substantial savings in weight and power (reduced from kilo-Watts per subsystem to tens of watts) can be achieved. We defined the improvements achieved by substituting SCE digital circuits for the GSTS TDP. The results are summarized in the figure. In addition to the quantified benefits shown, the producibility of the sensor is enhanced by the reduction of off-FPA cabling from 350 to approximately 50 (assuming use of SCE ADCs) and large decrease in parts count. The increased throughput available with SCE digital processing can be used to improve closely spaced objects (CSO) resolution, provide longer range target discrimination, and enhance ODP functions.

SCE Digital Processor Advantages for the GSTS TDP.



- Greater than 200:1 MOPS/LB advantage

	SCE	CMOS
Power (W)	6	2100
Weight (kg)	0.3	150
Size (L)	0.04	28

ELECTRICAL ENERGY
THERMAL ENERGY
GSTS WITH SEMICONDUCTOR ELECTRONICS
GSTS WITH SUPERCONDUCTOR ELECTRONICS

The 200:1 MOPS/LB advantage may be used to achieve lower payload weight or increased performance, or some combination.

This report summarizes the results of Phase 1 of the planned four phase program.

PHASE I-A: TECHNOLOGY EVALUATION

Phase I-A assessed the maturity of TRW's NbN SCE process technology and demonstrated the yield of digital building block components and devices. The yield assessment was derived from a database of parametric and functional test results taken over the temperature range of 4.2 K to T_C and correlated for chip-to-chip, wafer-to-wafer, and lot-to-lot effects. A 384 gate serial-in serial-out MVTL shift register was used throughout Phase I-A to provide real circuit performance for feedback to design and foundry optimization.

PHASE I-B: TECHNOLOGY VALIDATION

During the Phase I-B option, the existing 384 gate shift register served as a yield vehicle to validate the maturity of the NbN IC technology quantified in Phase I-A.

Shift Register Yield Vehicle Testing was carried out in stages using our automated circuit test stations. First, circuit characterization and functional test on individual gate and shift register cells provided quick turn-around data for fine tuning of the design and the fabrication process. Operating characteristics including bias margin were measured at temperatures from 4.2 K to 12 K and compared with design. Second, functional test of complete shift registers was performed to fully exercise their functions. The resulting go/no-go test data continued to be used to build a circuit yield database. Finally, high speed functional test of shift registers assessed high speed performance at temperatures from 4.2 K to 12 K. The high speed data establishes the baseline performance characteristics for a high speed NbN IR FPA DSP.

This project

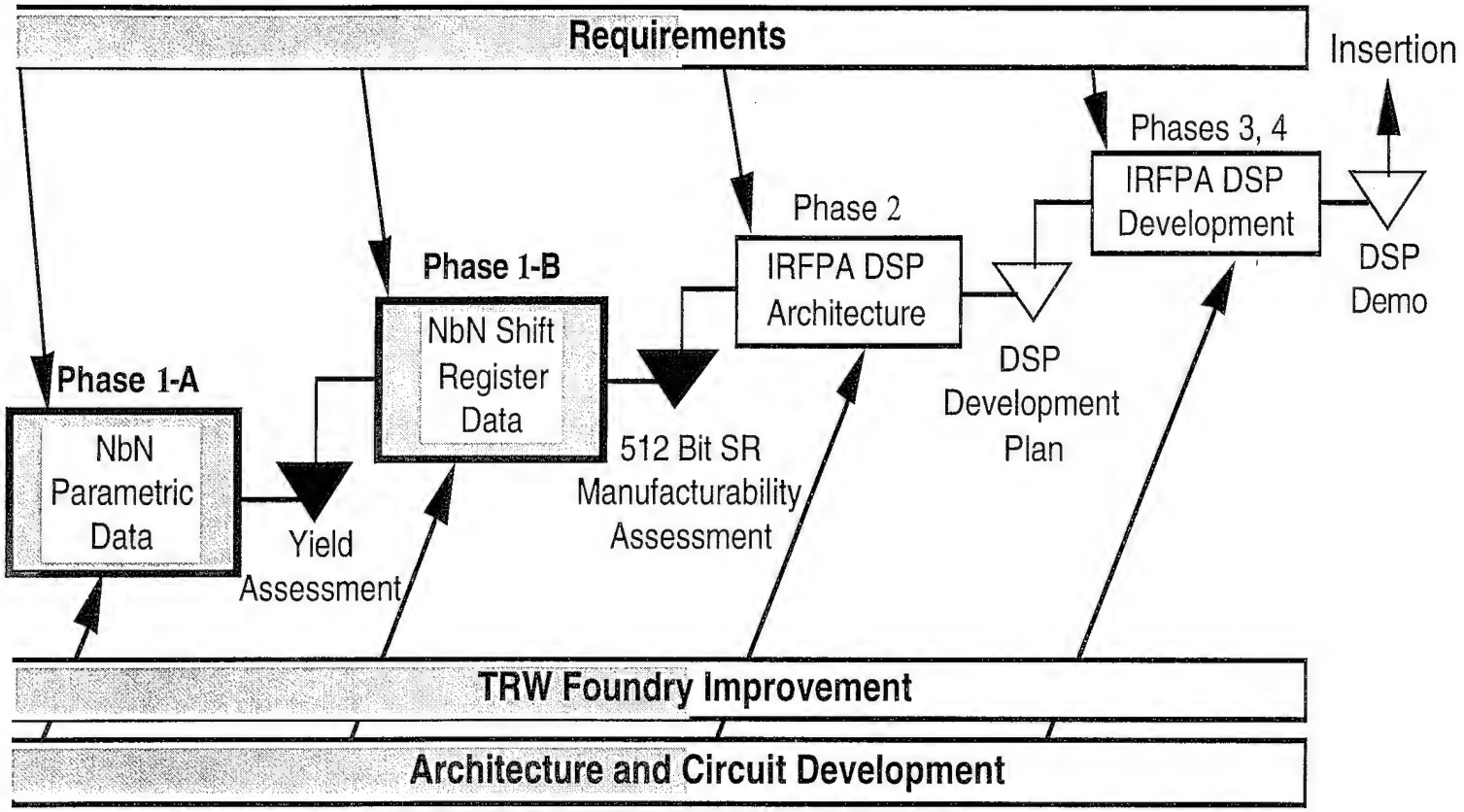
i) fabricated the basic devices and gates for a typical NbN digital technology,

ii) verified the spreads and temperature variations of the characteristics of these components, and

iii) compared these characteristics with those achieved for niobium device technology at the present time.

iv). estimated, based on these data, the resources that will be needed to bring NbN device technology to a level of maturity that will permit the fabrication of NbN digital chips with a gate count of more than 1,000 gates on a (nominal) 5 mm by 5 mm chip with an acceptable yield.

The First Phase of the Program Was Successfully Completed



Basic knowledge of NbN inductance properties were measured and used to layout a 384 gate shift register (SR) circuit. Experimental measurements of the circuit elements established that parasitic inductances associated with the junction vias resulted in unmatched products $I_1L_1 \neq I_2L_2$ for the MVTL gate. The design criteria requires $I_1L_1 = I_2L_2$.

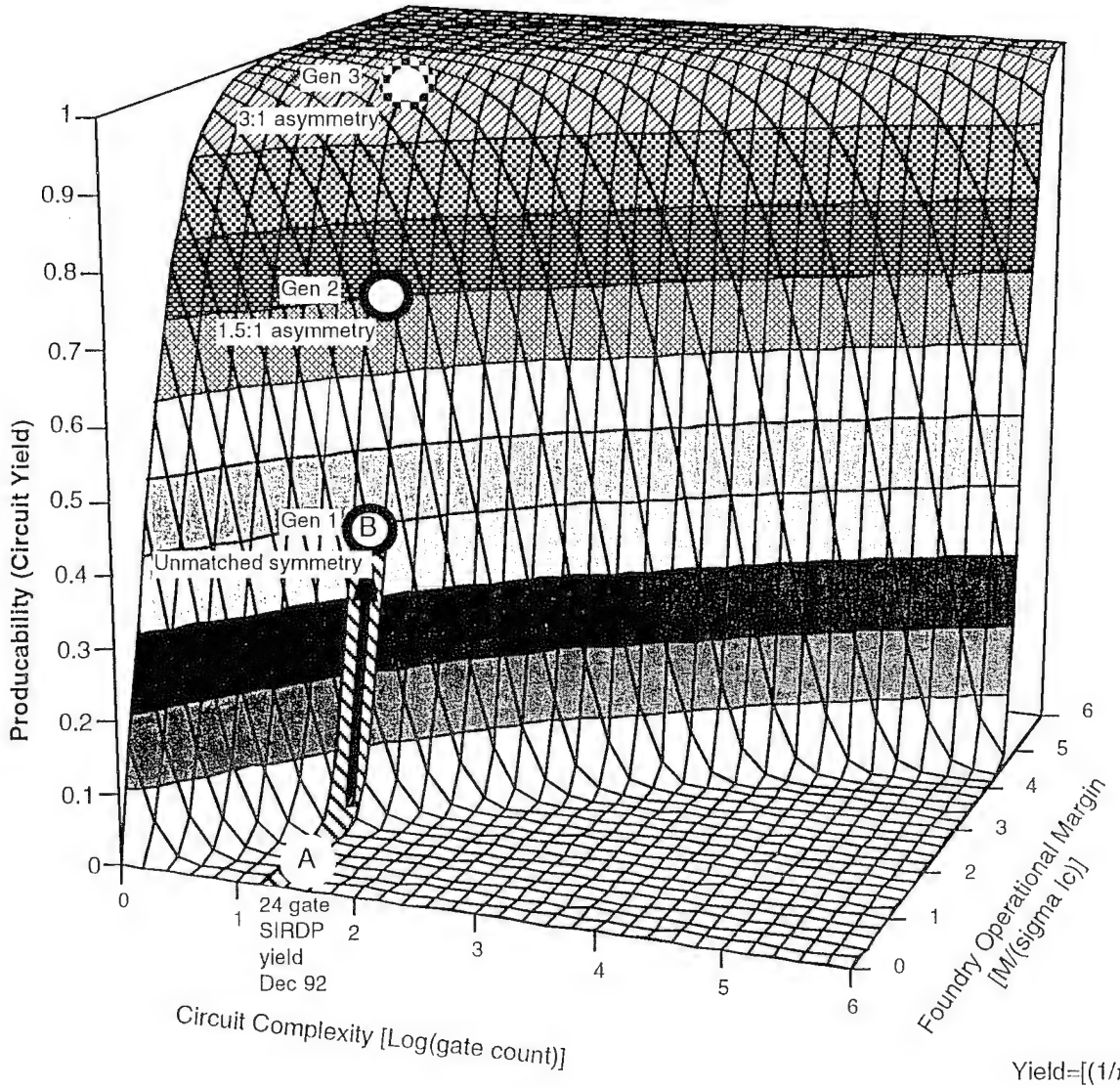
Generation	L Ratio	I_c Ratio	Circuit Yield	@ 10 K	@ 4.2 K
1	3:2	3:1	30%	Unmatched	
2	3:2	3:2	70%	Matched 110 gates	
3	3:1	3:1	≥ 90 %	Adjusted ratio for larger margins and more robust operation	100% for 800 gates

For the second generation logic cells, a quick fix of one mask adjusted the Ic ratio to match the inductance ratios. This modification significantly improved circuit yield.

A "design of experiments" cycle was performed which established the geometric layout required to achieve the 3:1 asymmetric inductance ratio desired for enhanced circuit performance margins. This 3rd generation design adjustment achieved further improvement in the circuit yield.

Based on these results, a 200 gate demonstration for another BMDO NbN project was selected as achievable within the performance and cost constraints.

NbN Design/Process Maturing at Rapid Pace



A. July 92 - First demonstration of a 10 K gate

Gen 1: October 92 - First demonstration of 24 gates at 10 K with 38% yield, quantified circuit inductance properties

Gen 2: May 93 - Demonstration of over 300 gates (quick adjustment of two of eight mask layers for 1.5:1 logic cell asymmetry)

December 93 - Demonstration of about 400 gates with around 74% yield (Additional runs with lower Jc trilayer wafers gave better match with the 1.5:1 asymmetry ratio)

Gen 3: May 94 - 90% yield of 24 gate circuits. Expect projected yield of 1000 gate circuits, operating at 10 K to be a usable 10% (Adjusted asymmetry to 3:1 for better margins)

$$\text{Yield}=[(1/\pi\sqrt{2})*\text{Integral}\{\exp(-x*x)\,dx\}]_{0}^{M/(\text{delta Ic})*\sqrt{2}}$$

The Process

Process descriptions and trend data quantify the maturity and capability of the Class 10 NbN foundry. We improved TRW's NbN circuit fabrication capability from single gate yields to yielding 400 gates in around 18 months. Trend charts provides an estimate of attaining 1,000 gate circuits with acceptable yields.

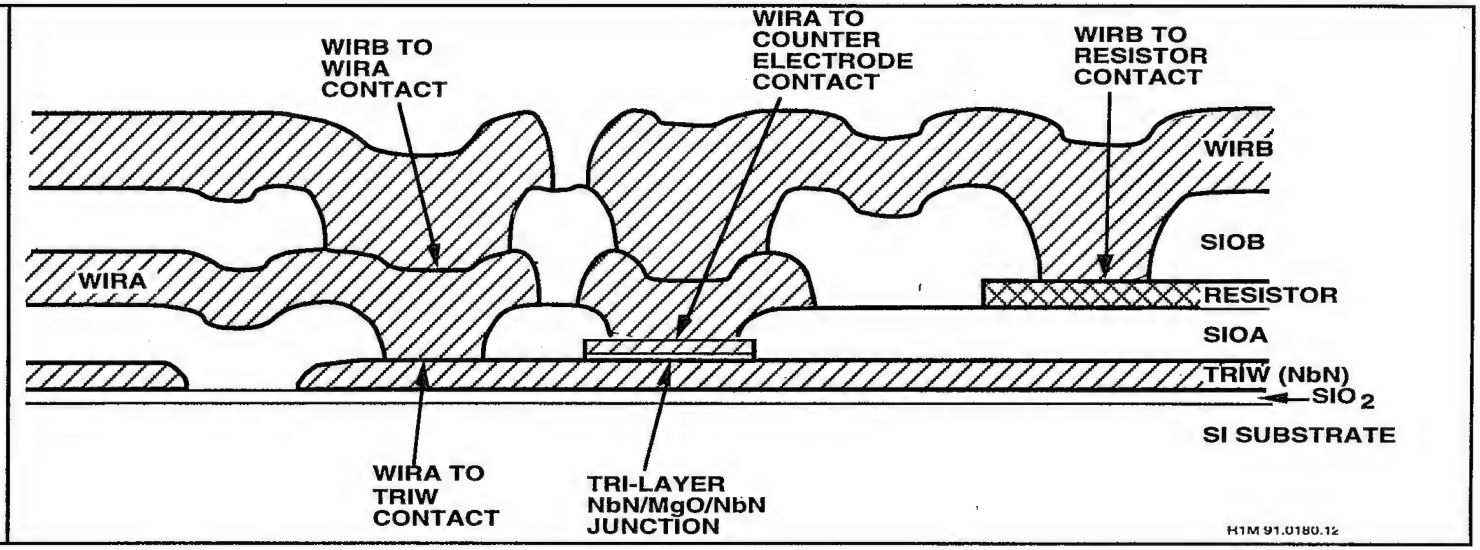
The Process

All the wafers for this program were fabricated using the JJ220 process, for which the design rules are provided in Appendix 1, and the cross-section is shown. The process features a NbN/MgO/NbN trilayer, three wire layers (NbN), a molybdenum resistor, two SiO_2 dielectric layers and a pin layer for bonding. All the layers are processed using reactive ion etching, except for the resistor and pin layers (which are patterned by liftoff). When the program started, the minimum feature was 3 μm for the contact via to a 5 μm minimum junction. During 1994, we developed a reduced scale of design rules (featuring a 35% overall reduction in footprint), in which the minimum feature size was reduced to 2 μm and the minimum junction size was reduced to 3 μm. These design rules support on-chip integration levels up to 1000 gates/chip. This latter effort was largely supported by TRW internal funds. The reduced design rule set is also given in the Appendix.

TRW Has Established a Fully Defined NbN-Based IC Process

JJ 220 NbN Process

- 8 masks
- 3 μm JJ
- 2 μm minimum feature
- 3 wiring layers
- 5 μm metal line pitch



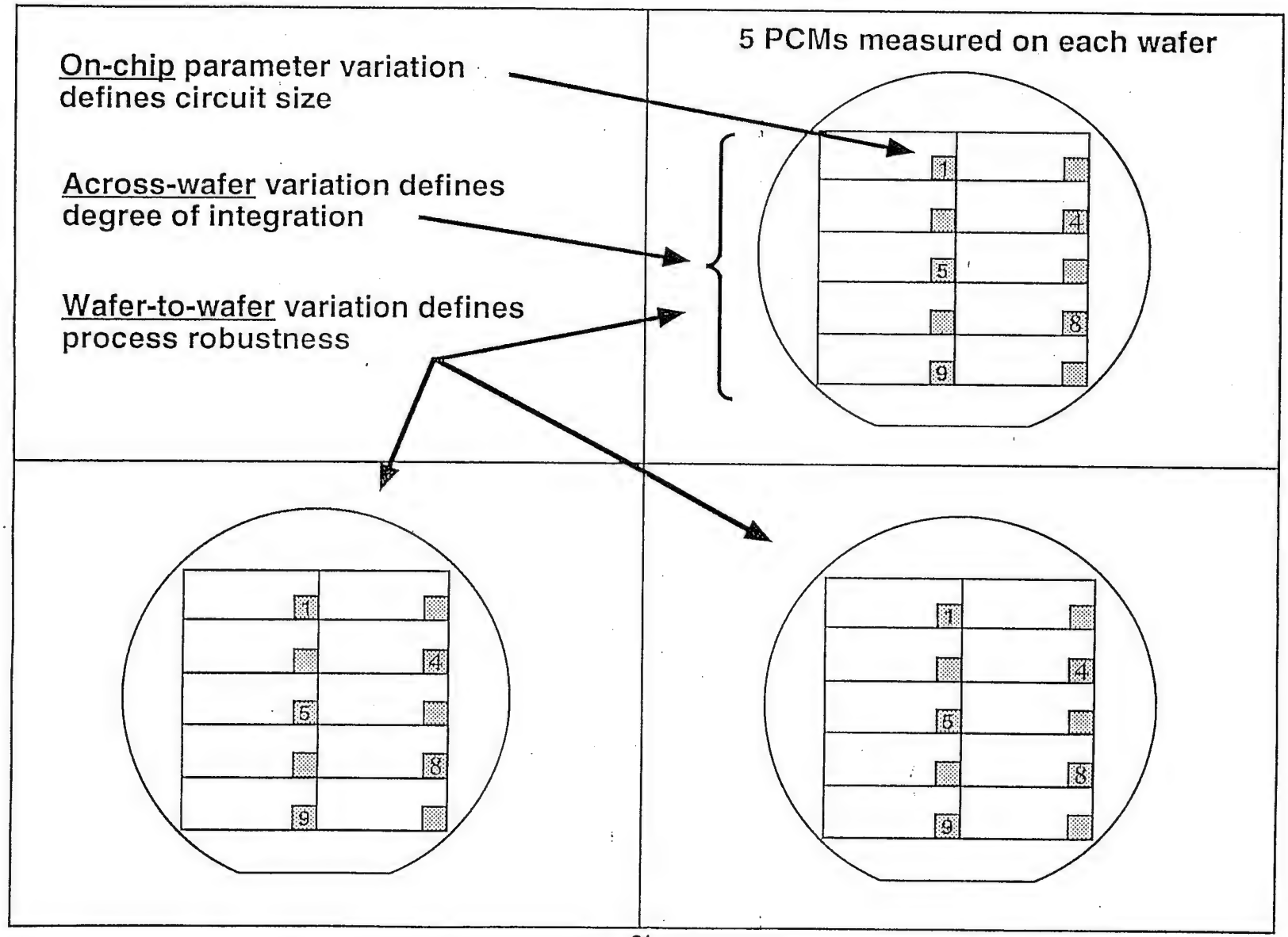
A substantial data base was established during the SIRDP program. We placed a standard process control monitor (PCM) test chip on every wafer that was fabricated through the foundry. The PCM contains an extensive variety of parametric test structures including junctions, junction arrays, resistors, resistor arrays, wire-to-wire contact arrays, capacitors, wire comb/meander structures and look-ahead devices. The table lists examples of the structures and parameters that were routinely measured. All of these structures are designed to verify the topological design rules and to provide an assessment of the wafer in terms of fundamental design parameters (e.g., junction critical current, resistor value).

Automated Testing Meets Program Requirements

Structure	Parameter	Variable Temperature	On Chip	Across-wafer	Wafer-to-wafer
Junctions	I_c (J_c)	√	√	√	√
	V_g	√	√	√	√
	V_m	√	√	√	√
	$I_c R_n$	√	√	√	√
Resistor	Sheet Resistance	√	√	√	√
Resistor	Contact Resistance	√	√	√	√
Contacts, Contact Strings	Contact critical current	√	√	√	√
WIRE Meanders	Wire critical current	√	√	√	√
WIRE Continuity	$I_{leakage}$ @ 1V	√	√	√	√
Capacitor	$I_{leakage}$ @ 1V, 5V (defect density)	√	√	√	√
SQUID	Inductance	√	√	√	√
128 bit, 3 phase MVTL shift register	Circuit operating margin	√	√	√	√

There are ten PCM chips located on every wafer as illustrated in the figure of which five are routinely measured to assess parametric device performance both on-chip and across-the wafer. We developed and used computer-automated testing capability during the SIRDP program, which included special test algorithms that allowed testing of all devices on the PCM in less than one hour. We also developed during the program a controlled temperature test capability that allowed automated testing of devices at temperatures between 4.2K and room temperature, with accuracy on the order of 0.1K. Since the implementation of variable temperature testing, we have measured every device at both 4.5 K (as a reference) and at 10 K (the operating temperature for the product circuits). Automated testing with automatic data storage drastically reduced the amount of time required for PCM (and product) testing and the test data in the computer, eliminating the time-consuming and error prone manual data entry. With this capability, we established an extensive data base involving over 100 parameters, tracking these for over three years, which allowed us to assess our process capability. The data base also allowed real-time feedback to the process team, providing faster problem-solving.

Uniformity and Reproducibility are Key Requirements for High Yield



We demonstrated process reproducibility and control in our NbN-based technology in several important areas. For the Josephson junctions, we tracked the junction characteristics (gap voltage, V_g, junction quality factor, V_m, and junction critical current, I_c) on every wafer fabricated, at both 4.5 K and 10 K. We periodically measured the temperature dependence of these parameters up to T_c to compare with device theory. Based on these data, we demonstrated excellent process control in both the gap voltage, V_g, and V_m at 10 K for our baseline process, as given in the table and shown in the trend charts in following two figures. V_m is a measure of the subgap leakage, and is calculated based on the product of the knee current and the inverse product of the leakage current measured at 3 mV (i.e., $I_{knee}*3mV*\pi/4/I_{leakage@3mV}$).

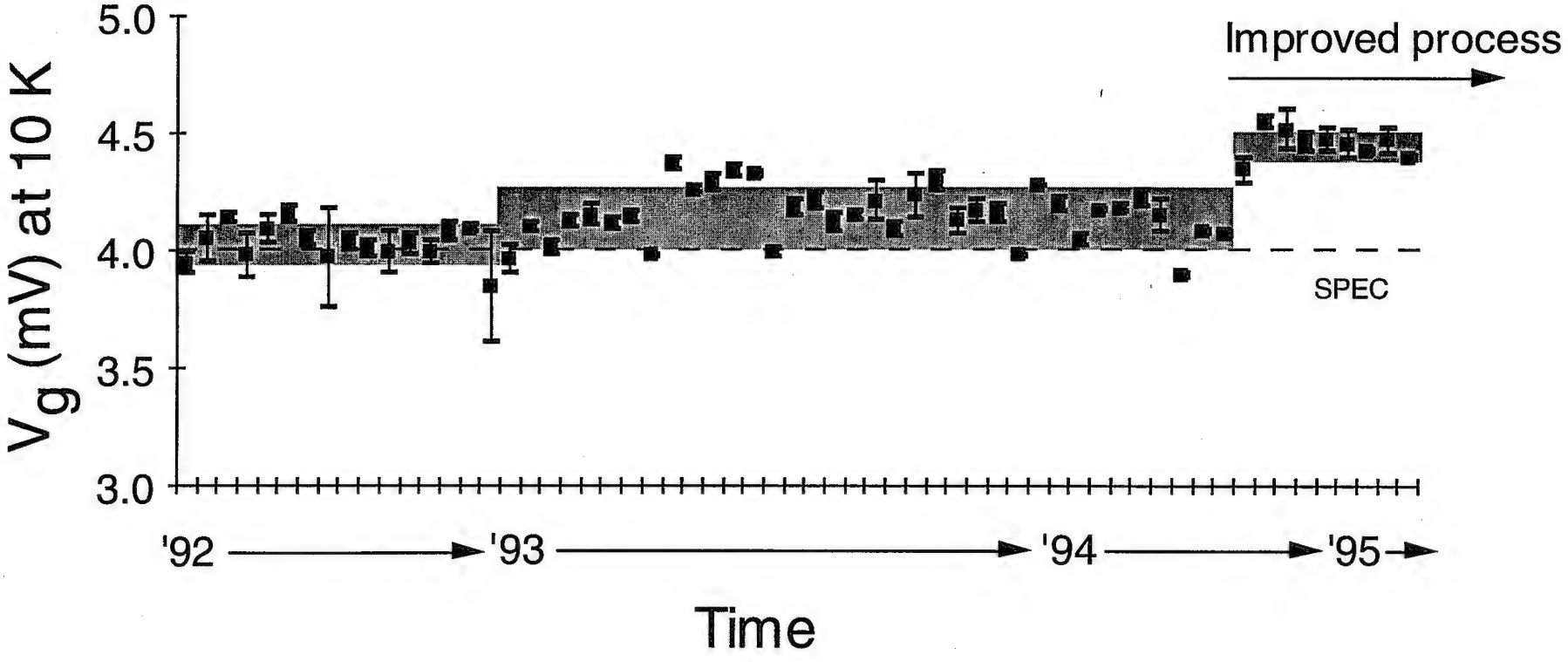
	Year	V_g (mV) @ 10K	V_m (mV) @ 10K
Base Line	1992	4.04 ± 0.06	11.18 ± 0.78
Project	1993	4.15 ± 0.12	11.78 ± 1.49
Project	1994	4.10 ± 0.10	11.09 ± 1.27
Post Project	1994/95	4.45 ± 0.06	15.38 ± 1.15

- Average values for V_g and V_m for 5 μm junctions were measured at 10 K on every NbN-based wafer fabricated during this program.
- Process control is better then ±3% for V_g and approx. ±10% for V_m.
- Other size junctions between 2 and 10 microns have similar characteristics.

Each data point on the trend chart represents the average and ±1 sigma of five measured values per wafer for 5 μm junction from the PCM chip at 10 K. When the 5 μm junction data was not available, another size was substituted (3 μm, 7 μm or 10 μm). As shown in this figure, the gap voltage increased by approx. 0.1 mV during 1993 and was extremely stable for the duration of the SIRDP program, controlled to better than ±3% variation. During the second half of 1994, we implemented an improved NbN junction process for which the measured gap value increased by 10%, approx. 0.4 mV, at 10 K. Achieved V_gs continue to meet or exceed the target requirements, a key enabler for 10 K circuit operation.

Consistently High Gap Voltage Means High Temperature Operation

Gap voltage is stable to within ± 3% for baseline process (V_g = 4.1 ± 0.1 mV) at 10 Kelvin



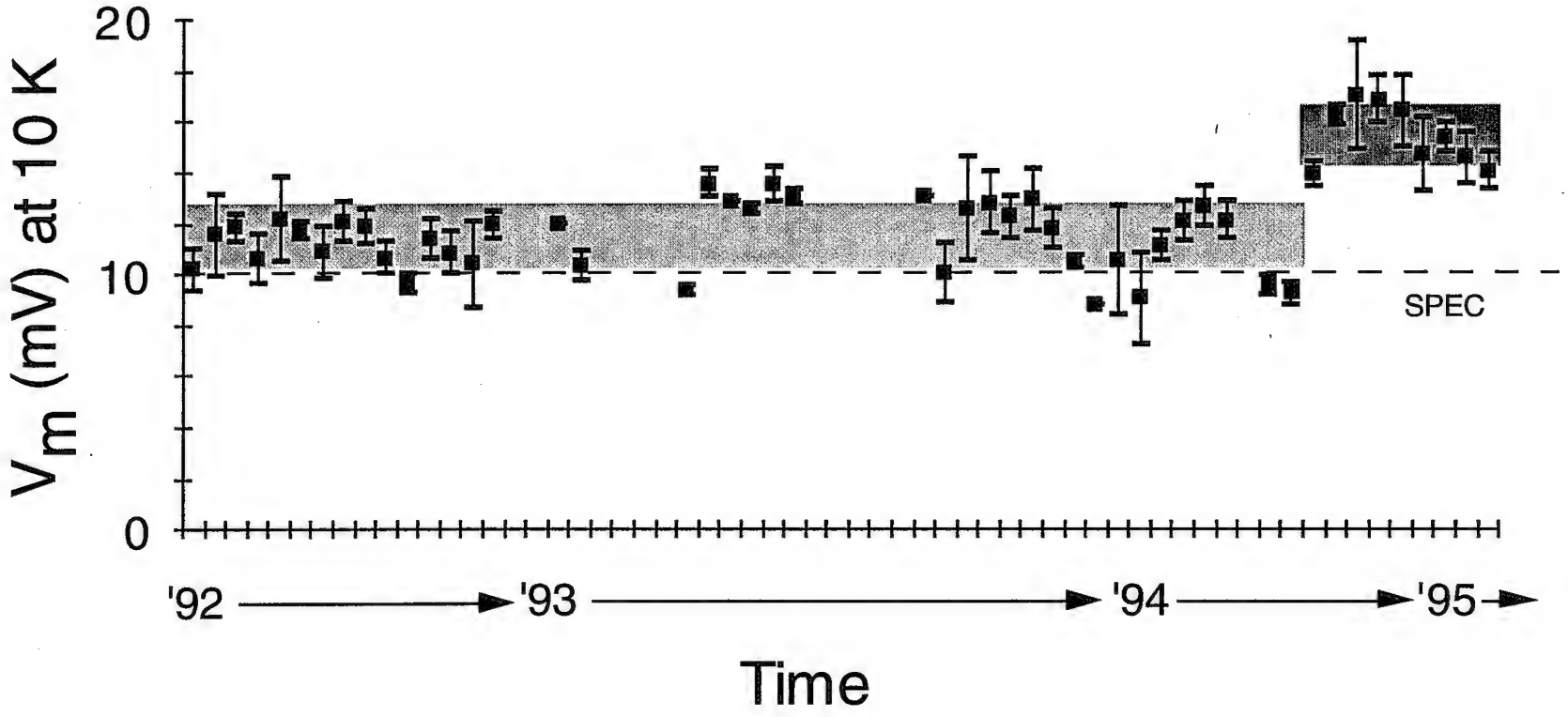
Improved NbN film process increases V_g by 10% at 10 Kelvin (V_g = 4.5 ± 0.1 mV)

Each data point on the trend chart represents the average and ±1 sigma of five measured values per wafer for 5 μm junctions from the PCM chips at 10 K. This chart shows V_m, for 5 μm junctions at 10 K, again demonstrating process control with slightly more scatter than for V_g. The increase in V_m in late 1994 is again due to the implementation of an improved NbN trilayer process, which resulted in a 35% increase, approx. 4 mV, in V_m at 10 K. V_m values continue to meet or exceed the target requirements, a key enabler for 10 K circuit operation.

Junction Quality Meets Circuit Requirement and Continues to Improve

TRW

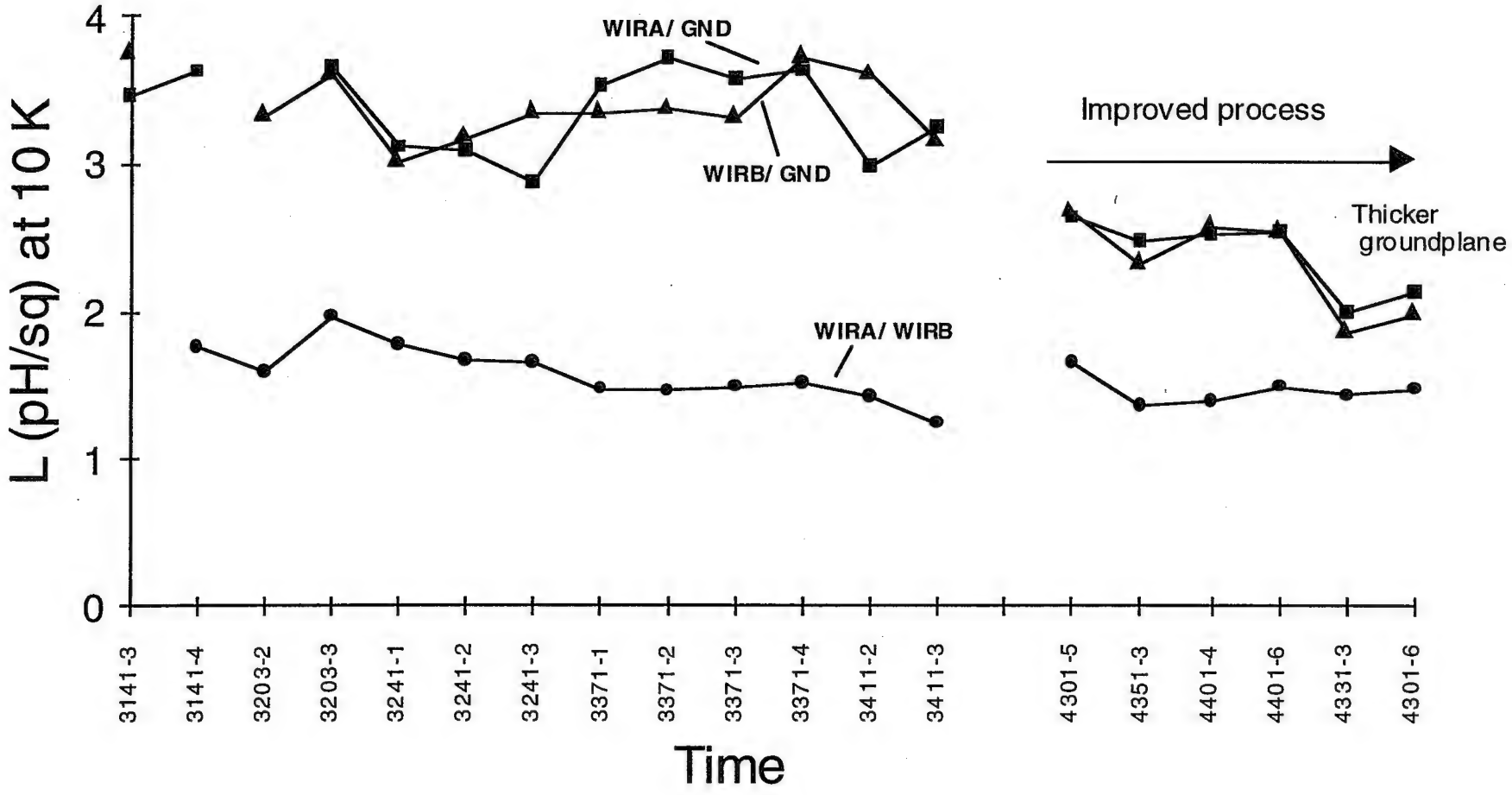
V_m is stable for baseline process ($V_m = 11.4 \pm 1.2$ mV)



Improved NbN film process increases V_m by 35 % at 10 Kelvin ($V_m = 15 \pm 1$ mV)

In addition to the standard PCM structures described above we implemented test structures to measure superconducting microstrip inductance for process control and circuit design during 1993. Microstrip inductance is extracted from SQUID measurements. The inductance test chip contains standard SQUID structures representing three different microstrip layout configurations: WIRA over GND (ground plane), WIRB over GND and WIRB over WIRA. Each configuration has four SQUIDs of different lengths. By measuring all of the SQUID inductances of one configuration, the common parasitic inductance due to layout constraints is eliminated, and the actual microstrip inductance per unit length is computed from a least squares fit of the measured inductance versus actual length. The London penetration depth is also computed from the inductance data and measurements of wire and insulator thicknesses. The inductance measurements were made on almost every wafer at both 4.5 K and 10 K since the structures were implemented. These are shown for the three wire combinations in the trend chart in the figure. As shown, the inductance per unit length (L/sq) was stable during 1993 and 1994. In late 1994, we improved our NbN deposition process, resulting in lower microstrip inductances as shown in the figure. A reduction of WIRA and WIRB inductance over ground plane by about 20% was achieved compared to the standard process. As shown, we also tested a thicker NbN ground plane (thickness twice the standard thickness) on selected wafers, which resulted in a further decrease in L/sq for an overall reduction in L/sq of WIRA over GND and WIRB over GND by 39% relative to the previous baseline process. Lower microstrip inductance reduces circuit parasitics and allows use of higher current density Josephson junctions for increased circuit speed.

Measured Inductance Values Demonstrate Stable Process at 10 Kelvin



Improved NbN film process reduces L/sq by 39%, enabling circuit design

This table lists the average and ± 1 sigma values for the measured microstrip inductance per unit length for the three wire pairs, for the standard and improved processes. The decreased inductance values contributes to easier circuit layout and higher circuit performance.

Process	WIRA/GND L (pH/square)	WIRB/GND L (pH/square)	WIRB/WIRA L (pH/square)
Prior	3.37 ± 0.30	3.39 ± 0.23	1.58 ± 0.20
Improved	2.54 ± 0.07	2.52 ± 0.15	1.46 ± 0.13
Thicker GND	2.06 ± 0.10	1.92 ± 0.09	1.45 ± 0.03

- Average values for microstrip inductance per unit length measured at 10 K for most NbN-based wafers fabricated during the SIRDP program.
- Process control is approx. ±10% for the standard process.
- The improved NbN film process reduces the WIRA and WIRB over ground plane inductance by about 25%.
- The thicker ground plane results in a further decrease in inductance by another 20%, or 39% overall.

We made many important improvements to the JJ220 NbN IC process during the SIRDP program. This table summarizes the process improvements that were implemented to improve parametric yield.

NbN Process Technology Continues to Improve

TRW

	1991 (220T)	1992 (SR1)	1993 (SR2)	1994
Successes	• Demonstrated NbN IC Process	• Demonstrated 10 Kelvin Operating Temperature	• Improved process yield: - Improved on-wafer variation in Mo resistor value to < 5% - Improved critical current targeting by 12 % over 1992 - Improved contact yield to nearly 100%	• Improved process yield: - Improved on-wafer variation in Mo resistor value to < 5% - Improved critical current targeting by 12 % over 1992 - Improved contact yield to nearly 100%
Actions	• Implemented Mo Resistor to improve contact resistance and sheet resistance targeting	• Implemented heated JJ process, improving gap voltage to 4.0 mV at 10 K • Implemented automated parametric testing	• Implemented SiO_2 RIE process	• Implement improved JJ process
Issues	• Low Wire Critical Currents • Poor junction critical current targeting • Non-uniform across-wafer junction critical current	• Poor Mo sheet resistance (R_S) targeting and large across-wafer variation in R_S • Low contact yield for liftoff process		• Low WIRB critical current • On-wafer and wafer-to-wafer I_C variation • Contact resistance (R_C) problem for NbN/Mo
Resolution	• Implemented Sloped Wire etch for improved step coverage	• Implemented wet dip prior to resistor deposition which reduced on-wafer variation (to < ±5%) and improved targeting to ±7% • Developed SiO_2 RIE process for improved yield	• Removed interface AlOx dielectric layer which reduced R_C to spec (< 0.2 Ω-μm^2)	
Related Progress	• Developed Heated JJ process	• Implemented variable temperature testing • Developed improved JJ process to reduce on-wafer and wafer-to-wafer I_C variation	• Developed NbN 12 Ω/sq. resistor, reducing MVTL OR gate area by 50% • Implemented gas shroud for MgO target to increase vacuum system up time • Implement inductance measurements on PC	• Improved dielectric using bias sputtered SiO_2

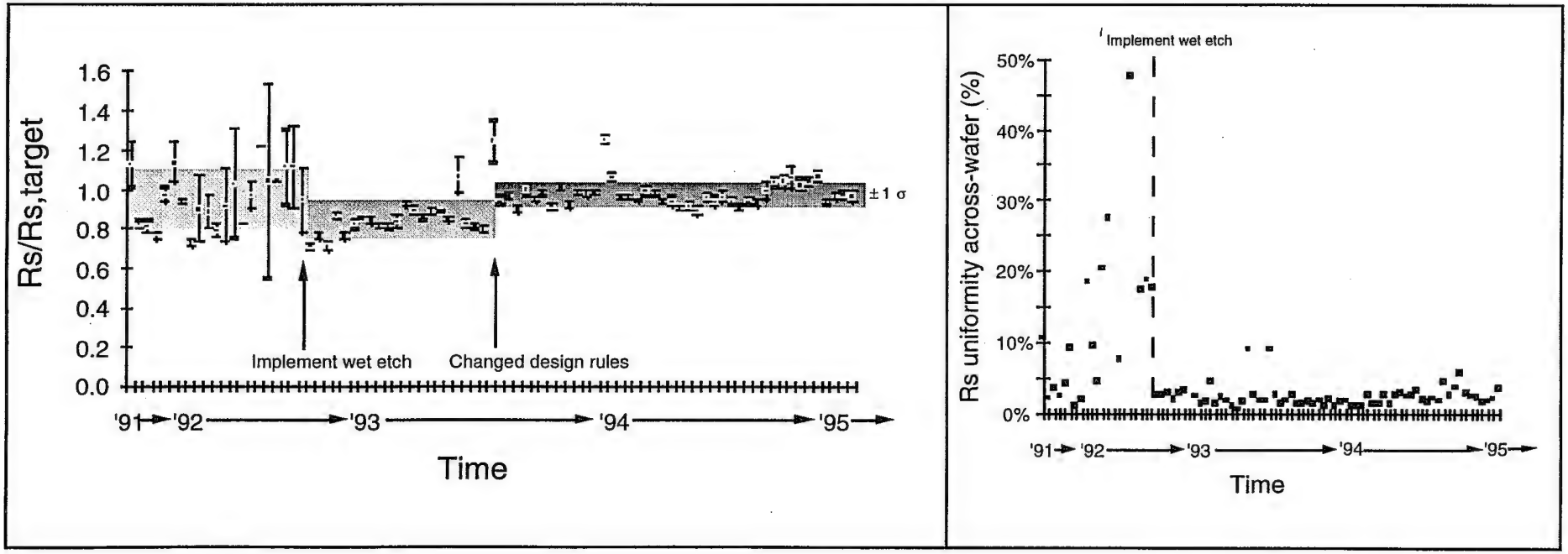
Resistor process: At the start of the SIRDP program, we implemented Mo resistors as a replacement for the previous TiAu resistor material to improve targeting and reduce contact resistance. In the early phase of SIRDP, we experienced on-wafer uniformity problem, which we solved with the implementation of a wet etch prior to Mo resistor deposition. This drastically reduced the on-wafer resistor variation and also improved the run-run variation. These effects are shown in the trend chart for the Mo resistor value. Each point represents the average and ± 1 sigma error bars for five measured values from the PCM test chip on every wafer, normalized to the target resistor value, measured at 10 K. After the implementation of the wet etch, the resistor value decreased and was stable for a series of many runs. Using standard statistical process control techniques, we then assessed process capability, which involved running a series of standard runs and determining the true process variability. (This technique can only be applied to a stable, in-control process). At this point the design rule was changed from a target of 1 Ω/sq to 0.8 Ω/sq to be in line with the established process capability (see wafers late '92 to mid '93). This was preferred to reducing the Mo thickness, which is presently at 70 nm. The result has been a stable process (3% below target on average, with ± 4% process variation) with good across-wafer uniformity.

Improved superconductive NbN film deposition process: We re-characterized the NbN film deposition process in 1994 to improve the film characteristics and address the run-to-run uniformity issues. These characterization efforts were supported by TRW internal funds and were carried out by a recently hired senior process engineer (on-board May '94). Following an extensive study to determine the important parameters affecting the deposition, several important system changes were implemented. These changes involved modifying the gas handling system, adding automated feedback control for the partial pressure of N_2 and hardware modifications to reduce plasma leaks and increase system up time. The net result is improved within-run uniformity, across-wafer uniformity and film properties, as shown above.

Process Improvements for Mo Resistor Results in a Stable Process

TRW

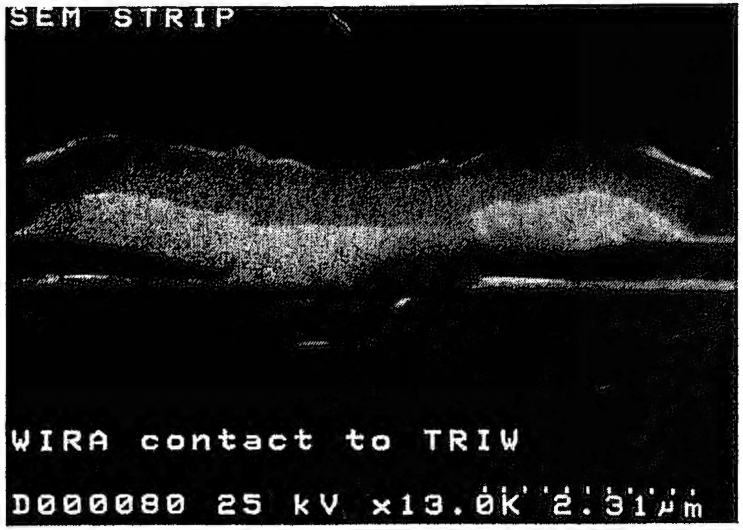
- Surface roughness is critical factor in resistor value
- Implementation of wet etch prior to resistor deposition reduced on-wafer R_S variation to < ±5% and improved targeting to ±7% in 1992
- Design rule changed after process capability assessment in 1993



SiO_2 etch process: We implemented a reactive ion etch (RIE) process for patterning of the inter-layer dielectric SiO_2, which replaced our previous baseline process which used a liftoff technique. We had experienced low contact yield on our PCM test chips, due to the contact via not lifting off. When the films are deposited by sputter deposition, which erodes and undercuts the photoresist profile, it is difficult to sustain a reproducible lift-off process. It is also not scalable to small feature size. In addition, even when the contact via does lift off, the edge is often sharp with remnant SiO_2 material, which makes NbN wire step coverage difficult. Both of these problems can lead to low contact yield.

We developed a RIE process to address these issues at the contact via etch step. The figure shows SEM micrographs that illustrate the nature of the problem. The mushroom structure seen in the upper right micrograph is the result of incomplete contact liftoff. The cross-section shown in the upper left quadrant illustrates the poor step coverage that can result at the contact edge (on the right side of the via) due to remnant material, even though the overall contact via profile is smooth.

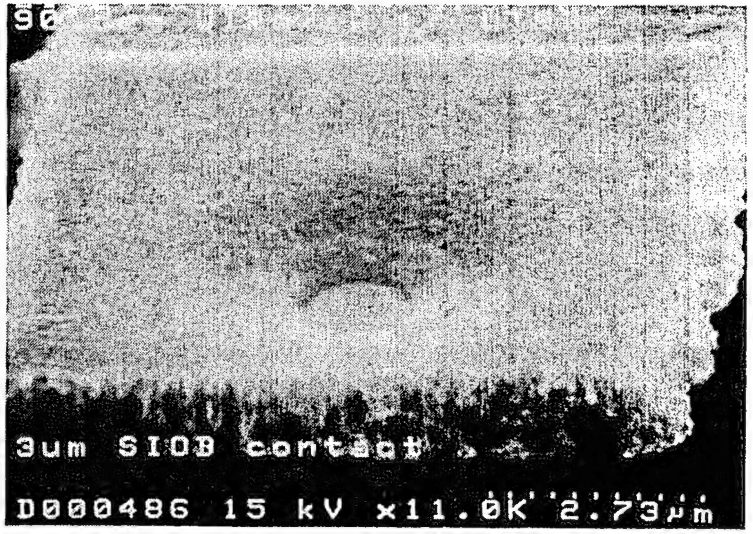
Problem: SiO_2 Liftoff has Low Yield for Small Contacts



CROSS-SECTION

POOR COVERAGE

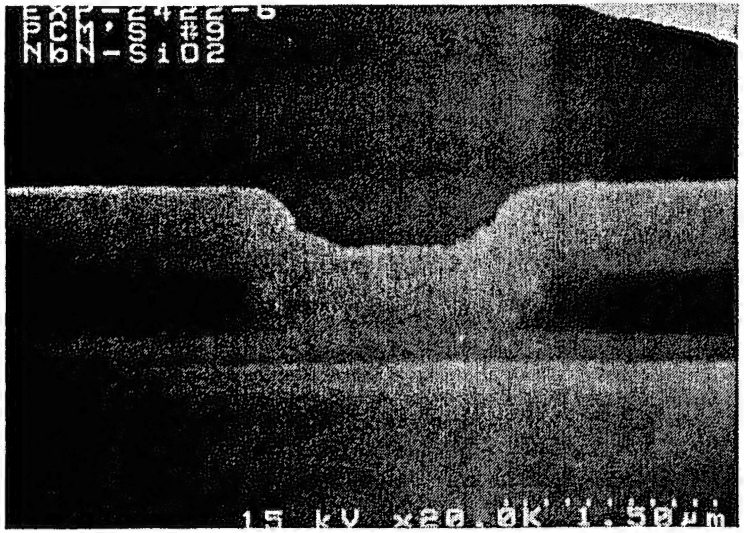
- Incomplete metal coverage leads to opens
- Contact and area shrinks from as-printed size
- Photoresist profile control becomes critical
- Low I_c for Nb/Nb contacts (<5 mA); poor yield for < 2.5 µm contacts



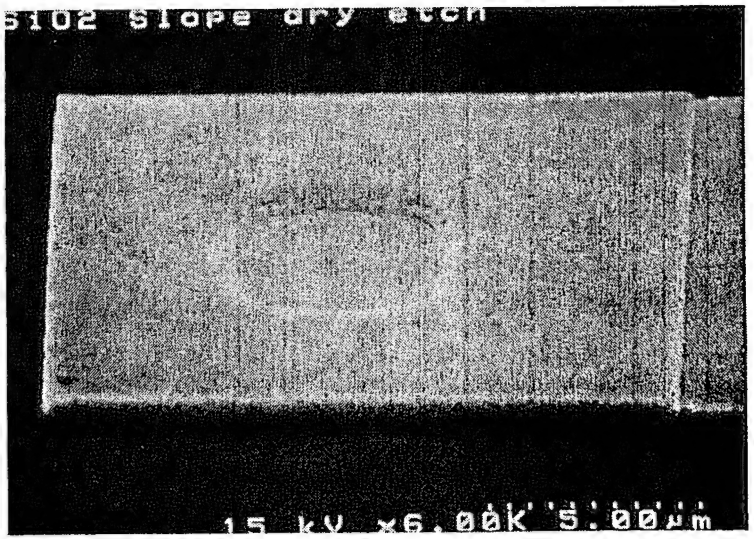
REDUCE WINDOW SIZE

This figure shows a good contact profile for contact vias defined by RIE. As shown, the step coverage is much improved and smaller features are obtained.

Solution: Dry Etching Produces Smaller, More Reproducible Contacts



CROSS-SECTION



5 µm CONTACT

- Sloped etch allows good metal coverage
- Contact size maximized and reproducible
- Excellent I_C for 1.5 µm Nb/Nb contacts (> 30 mA)
- NbN morphology limits contact I_C

1.5 µm CONTACT

This figure shows the PCM test results which we achieved for contact yield. With the liftoff process, we frequently experienced zero yield for series arrays of 100 contacts. After implementation of the RIE process, the yield has improved to nearly 100% and the measured contact critical current meets or exceeds the target specification.

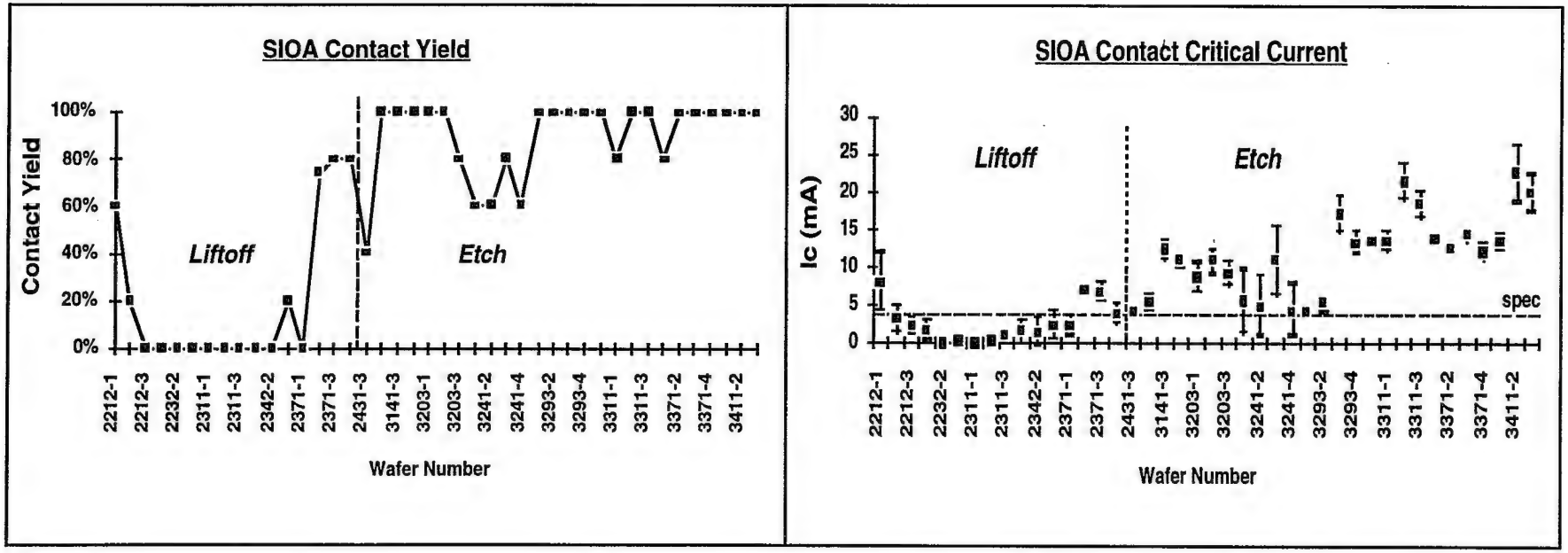
Wire step coverage: Another integration issue we faced in the early phase of the SIRDP program was the step coverage of the upper wire (WIRB) over the lower wire layer (WIRA). To improve the situation, we developed and implemented a sloped profile for the WIRA layer to facilitate WIRB step coverage. This process was developed using experimental design techniques. The previous process resulted in a nearly vertical WIRA profile, whereas the improved process showed WIRA slopes on the order of 40°. The net result was improved WIRB step coverage and increased current-carrying capability.

SiO_2 RIE Process Dramatically Improved Process Yield

TRW

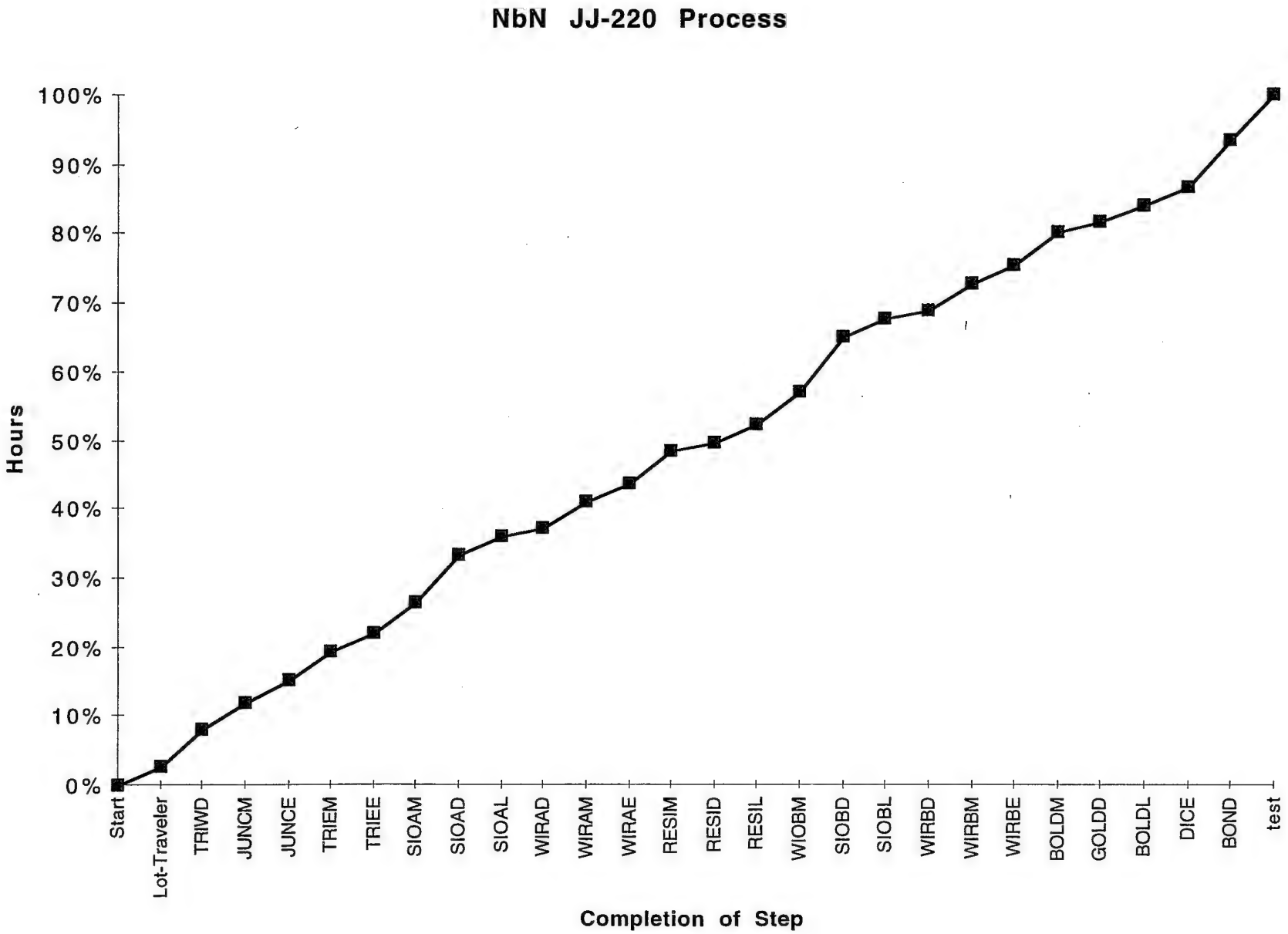
- SiO_2 reactive ion etch improved NbN process reliability and robustness
- Contact critical current improved by sloped contact profile

Parametric Test Yield and Critical Current for series arrays of 100 3 μm X 3 μm contacts



JJ 220 Process Flow Elapsed Time

The JJ220 is an eight mask process technology used for fabricating Niobium Nitride based integrated circuits. This figure illustrates the accumulated estimated percent of time required for each process step for running a wafer with this technology. It includes in-line process inspection, CD resolution, and alignment measurements.


NbN JJ-220 Process
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
Hours
Start
Lot-Traveler
TRIWD
JUNCM
JUNCE
TRIEM
TRIEE
SIOAM
SIOAD
SIOAL
WIRAD
WIRAM
WIRAE
RESIM
RESID
RESIL
WIOBM
SIOBD
SIOBL
WIRBD
WIRBM
WIRBE
BOLDM
GOLDD
BOLDL
DICE
BOND
test
Completion of Step

The Logic Cell

A logic cell building unit was established and refined, resulting in larger operating margins, hence higher circuit performance yield.

The Logic Cell

MVTL GATE FAMILY

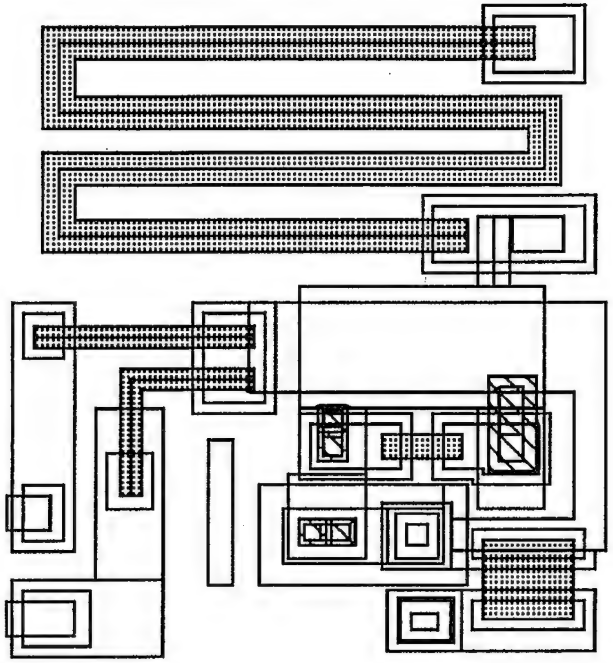
The objective is to attain improved margin and fan out for 10 K operation for complex digital circuits with gate count in the several hundreds (NbN) to the several thousands (Nb). The gates we use in our digital circuits are based on the "Modified Variable Threshold Logic" (MVTL) family. This logic family is based on an asymmetric dc SQUID that combines magnetic coupling with injection of the input signal current. The asymmetry improves the input sensitivity to a uni-polar signal, while the injection increases the modulation depth, hence bias current margin. For optimum operation, the asymmetry in the left-right inductances of the SQUID must be balanced by making the junction critical currents similarly asymmetric, such that $L_l I_l = L_r I_r$. For a given asymmetry, there will be an optimum β_L of the SQUID where the bias current margin is maximized. From modeling and analysis, a 3:1 asymmetry ratio was chosen as a trade between performance and manufacturability. In NbN, large specific inductances (inductance per square of the wiring layers) and large parasitic inductances (inductances not coupled with the control line) make the layout and design in NbN challenging.

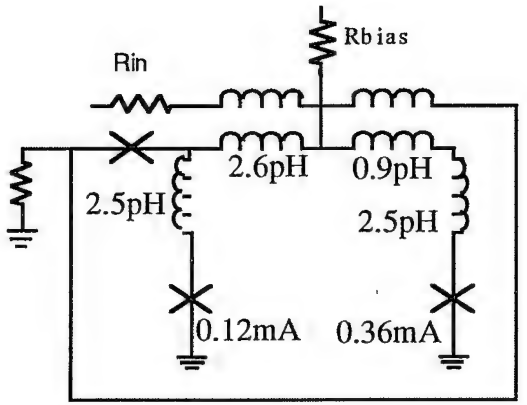
This figure is the layout of the initial design of the NbN MVTL OR gate, as translated from our established Nb gate library. The SQUID inductor in this layout takes into account the larger specific inductance of NbN (3.5 pH/sq. in NbN versus 0.6 pH/sq. in Nb). The larger specific inductance is due to many factors, including longer penetration depth, higher reduced temperature, (@ 10 K) and thinner base electrode thickness relative to the penetration depth (imposed by increasing surface roughness of thicker films). This gate is used in a ~400 gate, 3-phase shift register circuit for yield assessment.

An automated LabView™ test routine was used to measure over 20 chips in order to construct a preliminary statistical base for yield analysis. The margin is measured as the range of bias current over which the circuit operated. The fraction of working circuits is the yield. Yield data for this circuit is summarized as point A in the figure.

Analysis of the initial experimentally measured threshold curves of SQUIDs based on this NbN OR gate showed the presence of large parasitic inductances which skewed the left-right inductance ratio away from the intended ratio of 3:1 to a nominal value of 1.5:1. The critical asymmetry ratio was the designed 3/1 ratio. Further analysis attributed this parasitic inductance to current crowding at the junction vias. The extracted circuit schematic for this OR gate is also shown.

The Nb MVTL OR Gate Forms the Basis of the NbN Logic Family
This is the initial NbN layout as translated from the established Nb logic library.



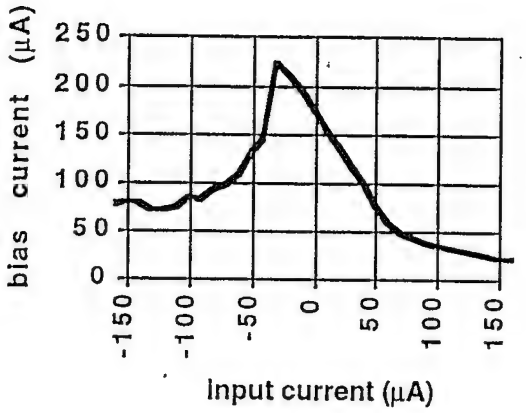


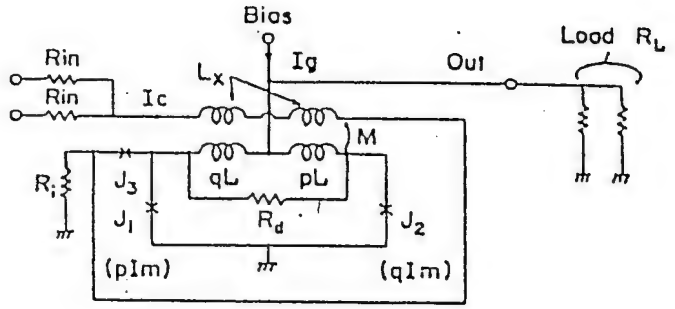
- Large inductance per square necessitates very compact layouts to satisfy design requirements.
- Lab data established that the measured inductance asymmetry was not the designed 3:1
- Modeling, supported by lab measurements, identified current crowding parasitic inductances of 2.5 pH per junction.

The first translation of the Nb logic "OR" gate cell into the NbN technology demonstrated well behaved characteristics to above 10 K. Performance margins and circuit yields are a function of temperature and decrease at higher temperatures. Although a few gates could be operated above 10 K, larger circuits operated at or below 10 K.

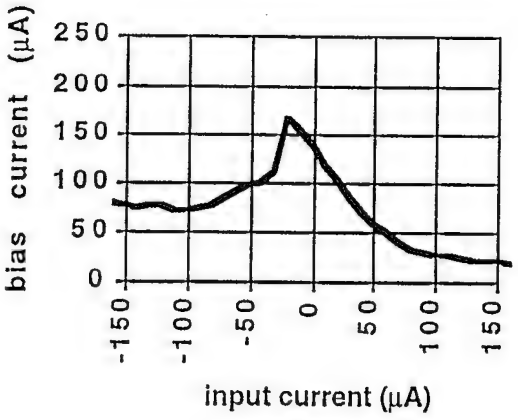
NbN MVTL Gate Characteristics are Well Behaved at 10K

8K

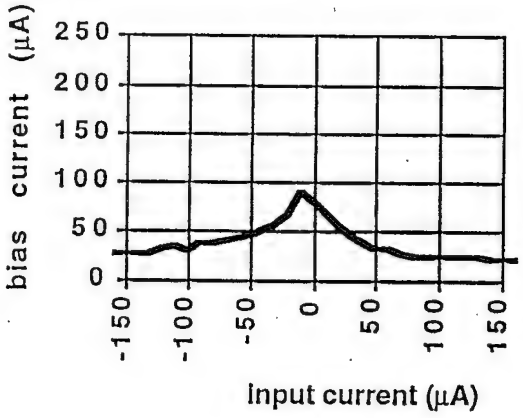




10K

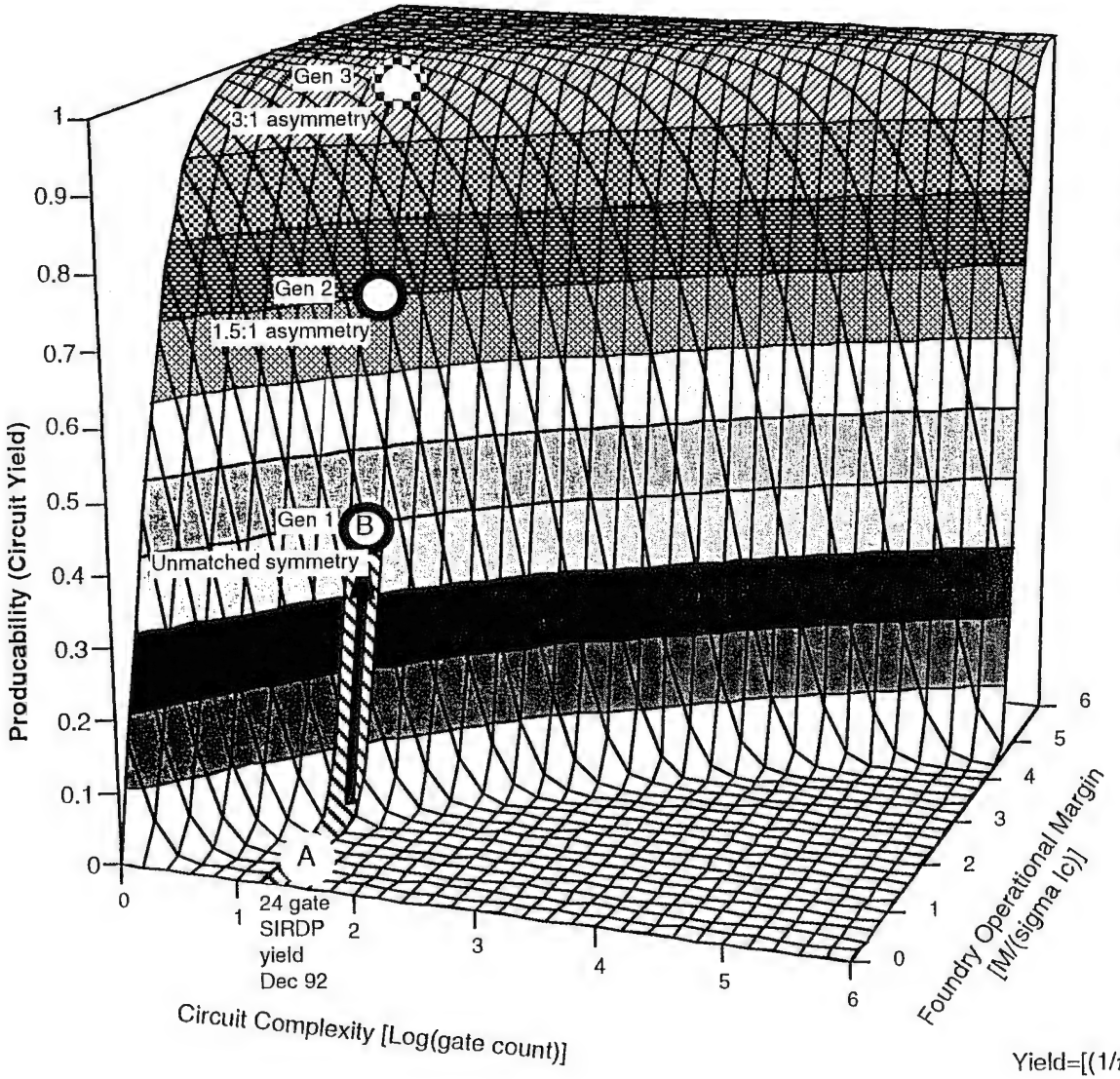


12K



To quickly assess whether the analyses of data and models were correct, the second step toward optimization of the gate margin was to make the junction I_C ratio 1.5:1 to match the inductance ratio. A two mask modification permitted this quick change providing design and modeling validation at low cost and quick turn-around. The predicted operating margin is 32 %, twice that of the unbalanced gate. The experimental results from the balanced 1.5:1 gate is indicated in the yield figure. This improvement in yield and margin was achieved as predicted but is still less than that theoretically attainable with the 3:1 ratio, where the operating margin is predicted to be about 37%.

NbN Design/Process Maturing at Rapid Pace



A. July 92 - First demonstration of a 10 K gate

Gen 1: October 92 - First demonstration of 24 gates at 10 K with 38% yield, quantified circuit inductance properties

Gen 2: May 93 - Demonstration of over 300 gates (quick adjustment of two of eight mask layers for 1.5:1 logic cell asymmetry)

December 93 - Demonstration of about 400 gates with around 74% yield (Additional runs with lower Jc trilayer wafers gave better match with the 1.5:1 asymmetry ratio)

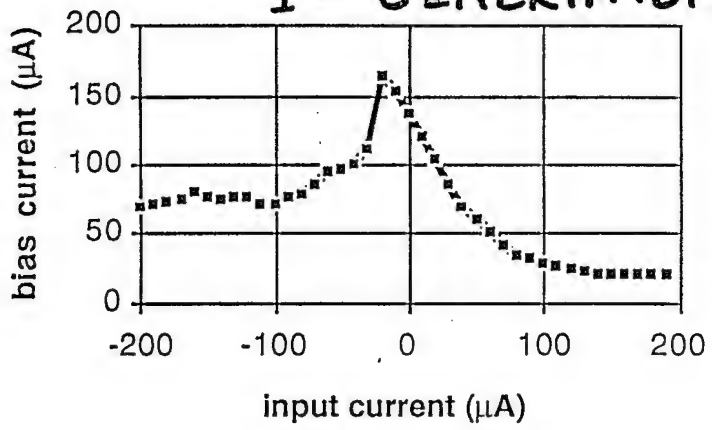
$$\text{Yield} = \left[\frac{1}{\pi\sqrt{2}} \cdot \int_{0}^{M/(\delta I_c)\cdot\sqrt{2}} \exp(-x \cdot x)\, dx\right]$$

yield chart mcdrw

The adjustment of the 10 K NbN critical current asymmetry to 1.5:1 to match the measured inductance asymmetry achieved the required equality $I_1L_1=I_2L_2$.. This change resulted in improved NbN threshold curve shape, coming closer to the established 4.2 K Nb gate characteristics.

SR1 design at 10K

1st GENERATION

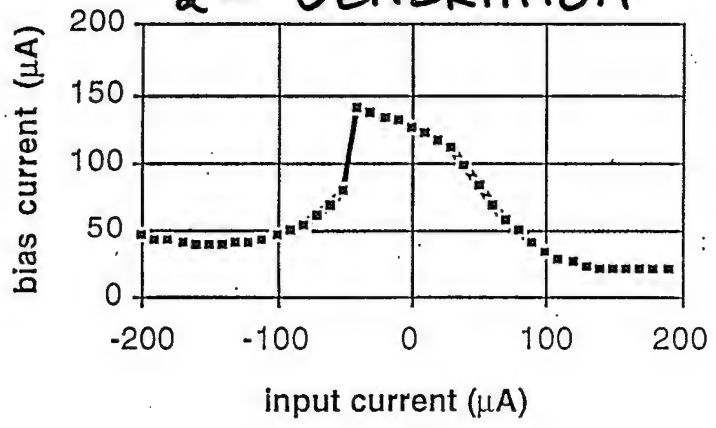


New gate design:

- threshold curve is closer to ideal
- gate is less sensitive to circuit parameters

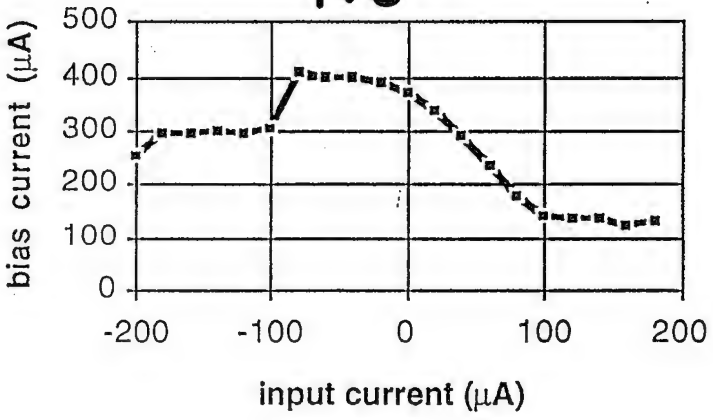
SR2 design at 10K

2ND GENERATION



Nb gate at 4.2K

Nb



OPTIMUM GATE LAYOUT

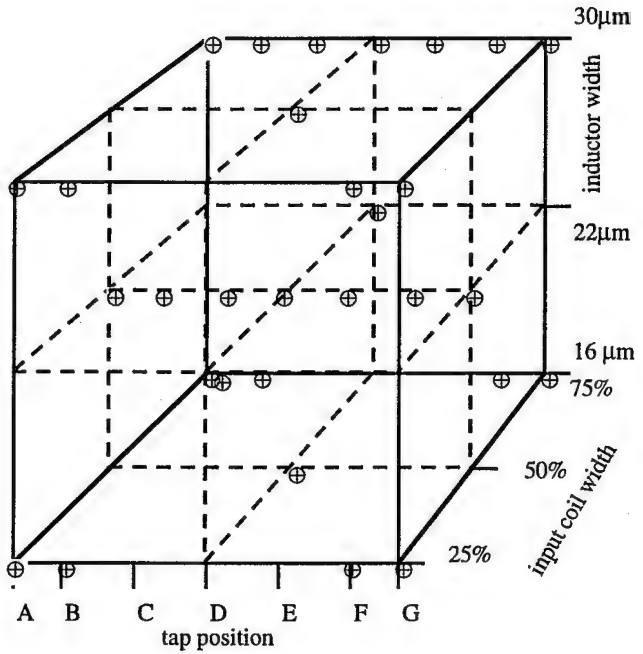
Determination of the position of the tap point to provide the desired inductance asymmetric ratio is complicated by the large parasitic inductance and complex current distribution.

The third step toward optimizing the gate was to empirically determine the layout that would give the desired inductance properties, in particular, the total SQUID inductance, the inductance ratio, and the mutual inductance. Based on the verified modeling equations, three parameters were varied: width of the SQUID loop (SQUID inductance), width of the coupling coil (mutual inductance), and tap position (inductance ratio). The junction areas, which are well defined by lithography, were fixed at the desired 3:1 ratio, with the small junction being 5 μm diameter, Additionally, the vias for both junctions were made the same size, to make the parasitic inductances (due to current crowding) equal. These parameter variations can be represented as the "experimental design cube" shown in the figure, where each axis is a parameter to be varied and each point represents a SQUID with the indicated values. The total number of variants was 30. Each of the 30 variants had 3 types of SQUIDs: magnetic coupling only, injected coupling only, and magnetic with injected coupling. The 3 types of SQUIDs provide duplication as a self-consistency check. For example, measuring the period of the threshold curves gives M, L_1, and (L_1+M), respectively, but each value can be determined with just two of the three SQUID types. Finally, each of the 30 variants had a full MVTL OR gate, to provide performance comparisons.

Chips from 3 different wafers were tested, such that each point on the cube was measured twice. This quantified the effects of wafer-to-wafer scatter, e.g., that due to variations in J_C. A total of 480 threshold curves were measured on an automated tester[1]; each of the 3 SQUID types and OR gates of the 30 variants of the cube were measured at 4.5 K and 10 K, from two of the three wafers.

[1]The measurements were performed in the TRW designed "Z-cryostat" which has very good temperature stability (typically ±.02 K), can be automatically controlled (here, by a LabView routine), and permits rapid sample swapping (typically less than 30 minutes to resume testing).

Design of Experiment "cube" provided a rapid acquisition of the needed design parameters



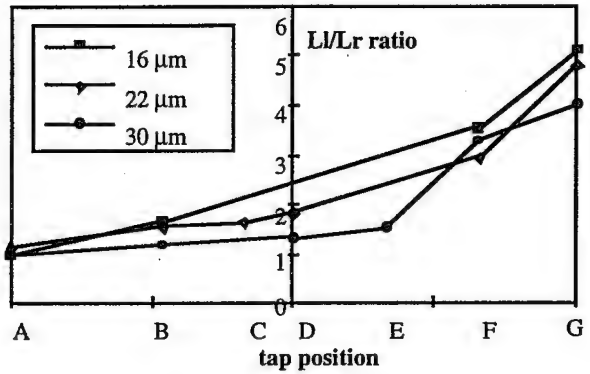
- Tap point "A" is the SQUID symmetry position, ($L_L = L_R$).
- Tap point "D" is the nominal bias tap position used in the initial translation of the gate structure into NbN.

Circuit parameters were extracted from the "design of experiment" data by computer fitting the threshold curves. This figure shows the extracted inductance ratio as a function of tap position for the 3 different inductor widths. The table summarizes the SQUID inductance and mutual inductance for each inductor width. From this data, we picked the point on the experimental design cube with 22 μm wide inductor and tap position "F" was selected as closest to the desired 3:1 inductance ratio (including the parasitic inductance) and smallest total SQUID inductance. Linear regression of the data can provide a predictive tool for designing to other criteria, and identifies which parameters affect a measurement most sensitively.

The parasitic inductances can be found by solving:

$$L_p = 0.5(L_{total}\ (2R/(R+1)) - 2L_I)$$

where $L_{total} = L_I+L_r+2L_p$ and R is the inductance ratio. The average extracted parasitic inductance is 1.4 pH $\pm$ 0.4 pH per junction via.



Total SQUID L and Mutual Inducance of the Control Line

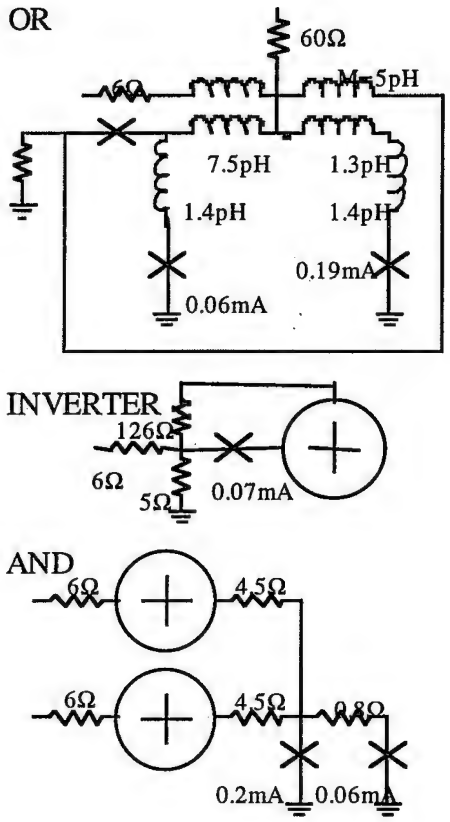
Inductor width	16μm	22μm	30μm
Total Loop Inducatance	13.3±0.5 pH	13.0±0.4 pH	12.1±0.8 pH
Control line width (as % of Inductor width)	Mutual inductance		
25% wide	5.4±0.2 pH	5.4±0.4 pH	3.6±0.3 pH
50% wide		4.5±0.1 pH	3.7±0.1 pH
75% wide	5.6±0.3 pH	4.6±0.1 pH	4.0±0.1 pH

- SQUID inductance ratio as a function of tap position.
- The three curves are for the three different SQUID inductor widths.
- The 22 μm inductor width is nominal value used.
- Nominal tap position F for the 22 μm inductor was used for the third cycle of gate performance enhancement.

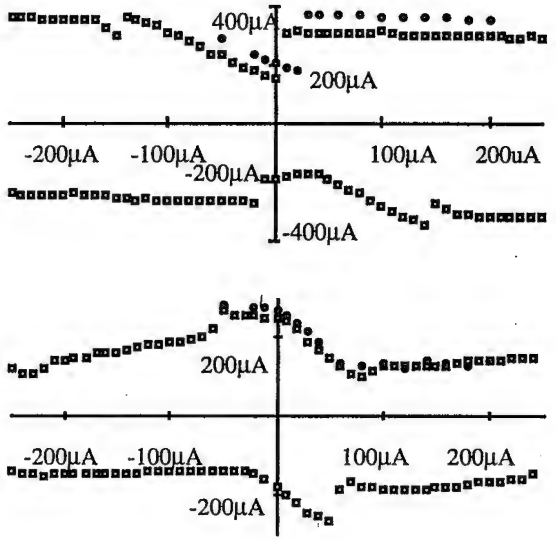
From the optimum NbN OR gate design, we constructed INVERTER and OR-AND gates. We used the margin analysis routine from JSPICE3 to vary circuit parameters to maximize the operating margin. The test circuit used in JSPICE is shown on the left. The INVERTER and OR-AND are simulated under fan out of 2. The "best" values for the parameters varied in the optimization are indicated in the figure. These gates were fabricated and tested. The measured threshold curves for these new INVERTER and OR gates closely match the SPICE threshold curve. The INVERTER margin is predicted to be 25 %, and the OR-AND margin is predicted to be 30 %, for fan out of 2 at 10 K.

The fourth step is to validate the new gate configuration. The newly optimized OR gates were used in an updated shift register circuit that is loaded to simulate a fan out of 2, to measure yield and margin. The approximately 400 gate circuit has yielded 100% at 4.5 K and better than 95% circuit design yield at 10 K based on the margin improvement, as also represented by "Gen 3" in the yield curve figure discussed earlier in this report (also see "yield" in later section). These yield values are for "design yield", a factor that includes the design robustness (e.g., margins) and process uniformity (e.g., J_C uniformity over the circuit). Presently, the process yield for the NbN technology is primarily a function of Jc targeting with nominal yield of 20 to 30 %. These two yield factors are multiplied to provide the expected total yield. Hence a 90 % "design" yield and a 20 % process yield would give an expected 18 % circuit yield.

Summary:
An efficient technique, often referred to as "design of experiment" was used to search a multidimensional parameter space in order to optimize a gate for high yield in complex circuits. Yield and gate count were improved from 38 % for a circuit with 24 gates (at 10 K) to 100 % for a circuit with 400 gates (at 4.5 K, 10 K measurements gave a yield of greater than 90 %).



Extracted values as determined by SPICE3, where the circles with "+" represents the "OR" gates.



Measured threshold curves for the Inverter (top) and OR gate (bottom). Solid points represent SPICE calculations of the threshold curves from the adjacent circuits.

The Results

The success of the program is attributed to the excellent, controlled foundry process, rigid, automated process control monitoring, and testing. A large quantity of laboratory test data provided statistical significance to the observed results.

The Results

A 128-bit shift register (384 "OR" gates) was used as an indicator of circuit yield

The figure lists a few of the factors that affect circuit yield. The first list are those factors for which the MVTL shift register yield vehicle provide data. The second are factors that were not within the scope of this contract to address.

None of the untested factors are expected to prevent the production of digital integrated circuits.

The MVTL buffer, or one-input OR gate, is the source of the logic family's gain and is responsible for the family's large margins. It is used in the AND and timed inverter gates. Building on the foundation of a high yielding buffer gate, constructing the complete logic family will be straightforward.

Superconductive digital circuit architecture and design focus on minimizing fan-out. In general, superconductive digital circuits will require some use of fan-out of two. We expect that circuits with fan-out of two will have reduced margins, and therefore reduced yield. Proper selection of the input resistors will minimize the effect of using fan-out of two.

The circuit yield measured using the yield vehicle chip on this contract includes the following critical factors:

- defect density
- connectivity
- process parameter spreads (Jc, Rs, and L) relative to the design sensitivity to these parameters

The yield vehicle chip does not test the following factors which could reduce the yield for general digital NbN integrated circuits:

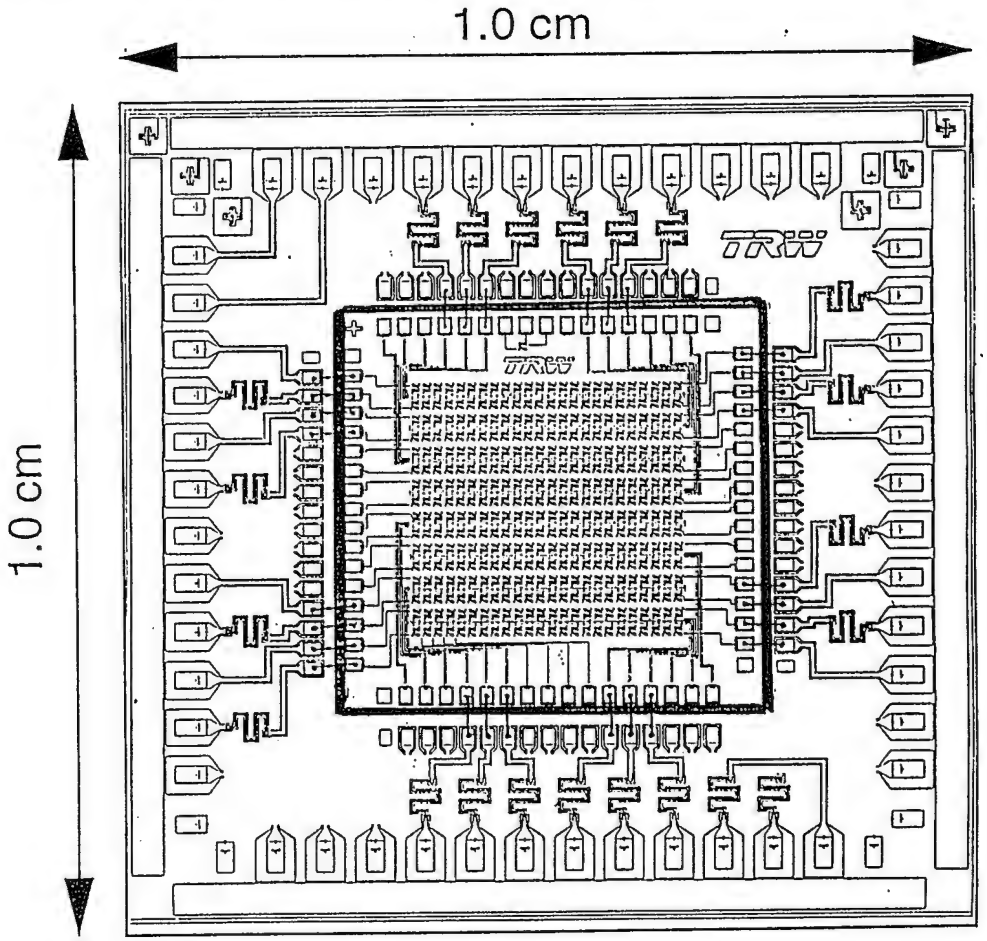
- gates other than the MVTL buffer (one input OR gate)
- fan-out greater than one
- high speed operation
- complicated topology (for example, routing signals back against the overall direction of the data flow)

NbN MVTL gates are intrinsically very high speed (the existing gates on this project are expected to operate up to a GHz clock rate, while those designed for higher J_C should operate to 5-10 GHz).

As an expedient demonstration, a section of a low speed yield vehicle chip was operated at 167 MHz. To expedite this test, the 0.5 cm shift register chip was mounted within a 1 cm printed circuit board "carrier" as shown in the figure. This 1 cm board was then inserted into TRW's thermally controlled high speed test probe and the test performed.

NbN Shift Register Chip Adapted to High Speed Variable Temperature Probe

- 10 Kelvin operation
- data taken to 167 MHz
- chip is bonded to intermediate carrier
- carrier fits in 56 pin high speed probe

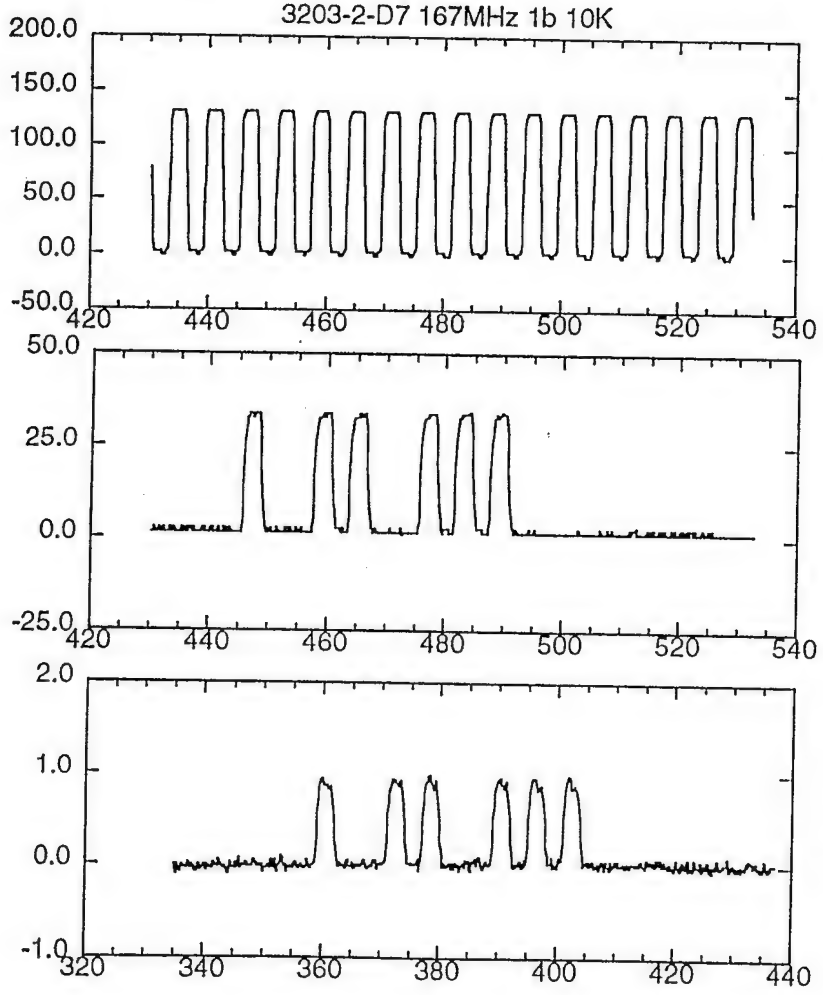


High speed test results are illustrated in this figure. The rise and fall times of the output signal indicates that this circuit could have operated several times faster if the appropriate high speed clock and I/O package were available.

Implementation of standard superconductive circuit high speed packaging will easily increase this speed several fold. The reduction in circuit operating margin with speed in the 100 MHz to 1 GHz range is primarily due to difficulty in delivering the clock/power to the gates.

Complicated routing of signals is not expected to degrade circuit performance in the 100 MHz to 1 GHz operating range but may become a concern at higher frequencies. The superconducting ground plane present on our chips is expected to provide a very high degree of isolation between signals on-chip.

NbN Shift Register at 10 Kelvin, 167 MHz



- clock/power phase 3
- input pattern
- output pattern

Yield Measurement Results for the Third Generation Gate Design

One lot of four wafers of the circuit tooling containing the third generation NbN MVTL buffer gates was fabricated. Circuit yield chips from this lot were tested to provide verification of the yield predictions for the third generation gates. These chips provide the best data set from which to predict yields for 1000 gate circuits.

The target Jc was 300 A/cm^2 (at 10 Kelvin). The measured wafer Jc values for the four wafers are shown in the table. We had previously shown that the circuit yield is greatly reduced for chips that are not between 0.5 and 1.5 times the target Jc. The Jc values of wafers 4121-1,3, and 4 are outside this range, so wafer 4121-2 was used to provide a test of our yield predictions for the third generation gates.

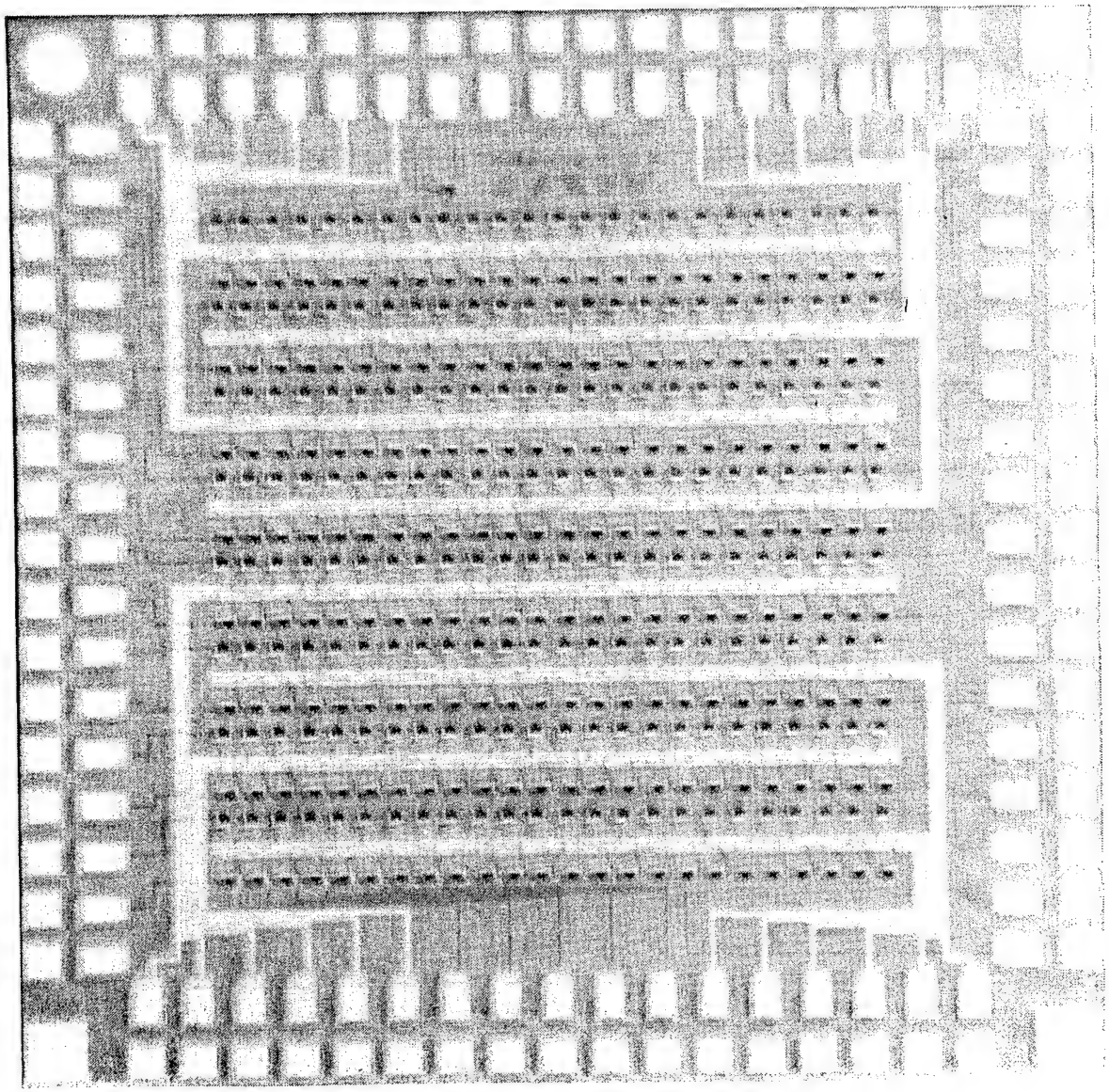
Third Generation circuits with asymmetry ratio of around 3:1.

Wafer Number	Circuit Tooling	Target Jc	Measured Jc	Measured Rs
4121-1	3rd generation	300 A/cm^2	550 A/cm^2	0.79 Ω/sq
4121-2	3rd generation	300 A/cm^2	325	0.78
4121-3	3rd generation	300 A/cm^2	734	0.75
4121-4	3rd generation	300 A/cm^2	669	0.75

- One wafer in four had targeted Jc giving a process yield of 25 %.

The yield vehicle chip contains sixteen independent shift register sections. Each section consists of 24 NbN MVTL buffer gates in series. The clock/power signal is delivered to the gates in three phases giving the circuit a memory capability. All gates in a section must function correctly for the correct digital pattern to pass through. The yield testing for the third generation gates was completely automated. The test station used an algorithm to search for the operating margin of each shift register section. If no operating region was found, a zero was entered for the margin, and the section under question is considered a non-yielding section. The number of yielding sections divided by the total (sixteen) gives the measured yield of 24-gate sections.

384 Gate, 10 Kelvin, NbN Serial–In, Serial–Out Shift Register



Interpretation of the yield data is complicated by an environmental/testing effect common in superconducting circuits, known as flux trapping. The effect is manifested here as a statistical localized failure of gates on the same chip from one thermal cycle to the next.

Under certain conditions at the time a superconductive integrated chip is cooled through the superconducting transition, magnetic flux can become trapped in one of the superconducting films. A flux quantum trapped near an MVTL gate can cause that gate to fail. Cycling the chip in temperature to release the trapped flux will cause the gate to recover and function correctly again. Flux trapped somewhat farther from the gate can also cause the gate to function with a reduced margin.

Standard techniques were used to reduce flux trapping as much as possible within the time and cost constraints of the project but did not completely eliminate the effect on the data. We were able to separate some of the yield reduction due to flux trapping from the "true yield" (that which one would measure if flux trapping were eliminated). Assuming that the process is random, the yield derived from measuring the same chip a number of times will approach the true yield. If a given shift register section operates on at least one thermal cycle it is counted as a yielding section in a composite yield. This procedure can only give a lower bound on the true yield because it does not eliminate the possibility that a preferential flux trapping site is located near a gate resulting in a failure on any number of consecutive thermal cycles.

Each chip was thermally cycled three times while measuring the operating margin of all sixteen shift register sections in each cycle. The yield of 24-gate sections for each test is listed in the table along with the derived composite yield. The total composite yield for the four chips on this wafer is 100%. Taken collectively, the four chips contain a total of 1536 gates.

Results of 3rd generation shift register yield tests are very good.

	4.5K data				9.0K data				10 K data				
	1st cool	2nd cool	3rd cool	4.5K comp	1st cool	2nd cool	3rd cool	9.0K comp	1st cool	2nd cool	3rd cool	10 K comp	total comp
B10	94	100	100	100	63	75	63	81					100
D5	100	100		100	69	75		75	38	31	31	50	100
F10	94	94	94	100*	44	56	63	75					100
H5	94	94	100	100	63	81	75	88					100

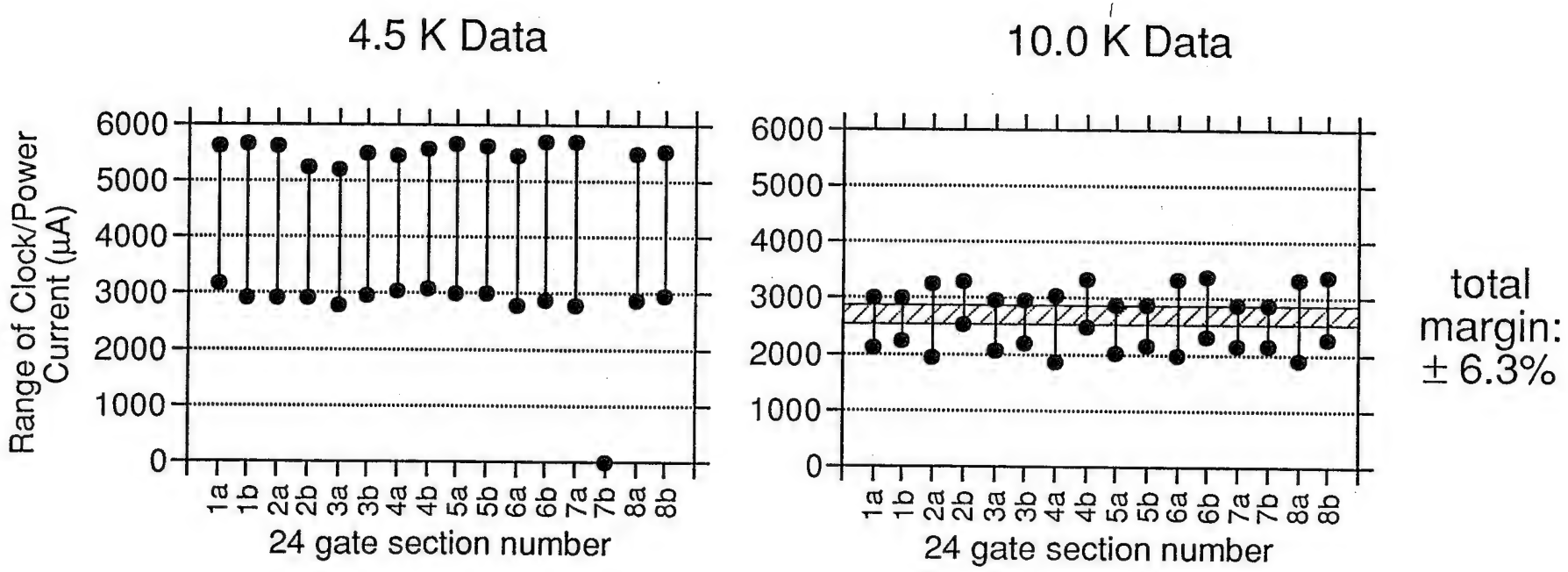
* Different stages did not operate on each cycle. Hence flux trapping was attributed to causing only 94% operation on each cycle.

- 100 % composite yield (i.e., excluding flux trapping) at 4.5 K.
- Over 75 % composite yield at 9 K.
- Around 50 % composite yield at 10 K.
- We expect that refinements in the circuit design, combined with techniques to reduce flux trapping will produce functional 1000-gate, 9-10 Kelvin, NbN, digital circuits using our existing fabrication process.

The second generation circuits ($I_L/I_R = L_R/L_L$ = 1:1.5) resulted in full operation of the 384 gate "yield" vehicle at 10 K. The full circuit margin was ± 6.3 %.

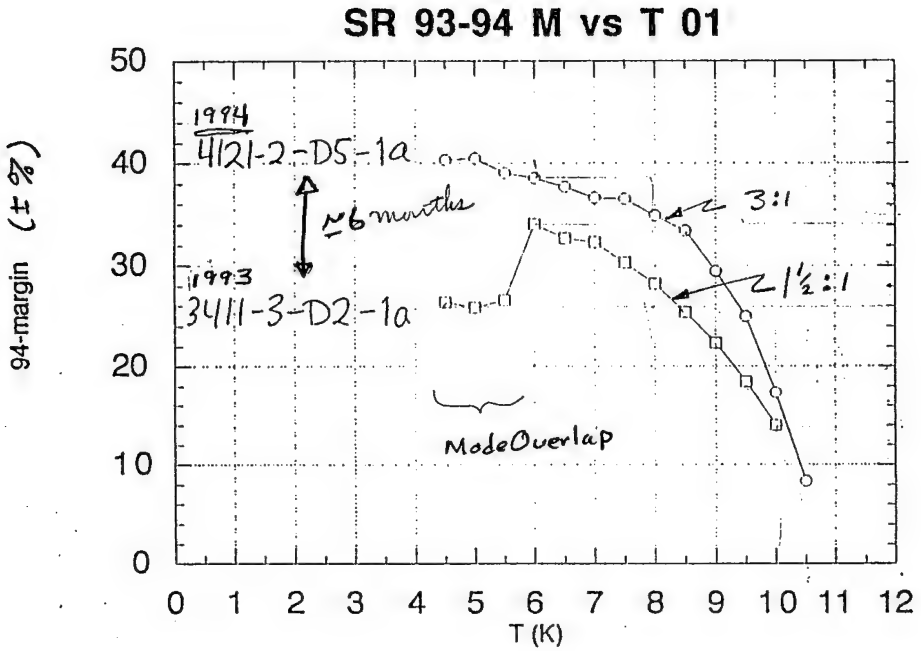
Moving the asymmetry ratio from 1:1.5 to 1:3 improves this margin.

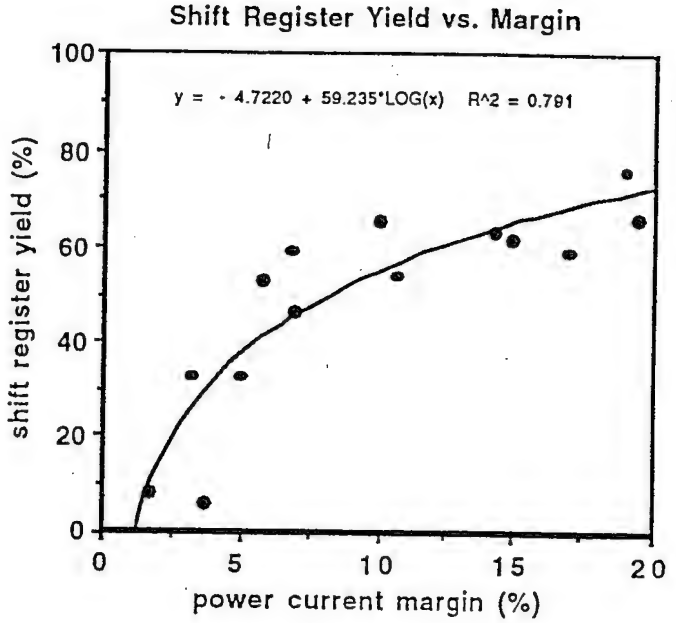
Fully Functional 384 Gate Shift Register Demonstrated at 10.0 K using Second Generation Gate Design



The left figure summarizes the margin improvement achieved when the "OR" gate asymmetry ratio was "optimized" to the 1:3 ratio from the 1:1.5 ratio. At 10 K, this represents a 26 % improvement, at 8 K a 25 % improvement and at 6 K, a 14 % margin improvement. This improvement was achieved in a 6 month period.

The right figure shows the correlation between circuit yield and clock/power current margin. Even with all the other possible yield limiting factors (e.g., open or short circuits) randomly distributed throughout the data, the correlation between yield and the clock/power current margin is strong. This is most likely due to the sensitivity of the gate design to spread in Josephson junction parameters. The primary thrust has been to improved the gate design to reduce its sensitivity to variances in the junction parameters.


SR 93-94 M vs T 01
94-margin (± %)
T (K)
1994
4121-2-D5-1a
~6 months
1993
3411-3-D2-1a
3:1
2 1/2:1
Mode Overlap
0
10
20
30
40
50
0 1 2 3 4 5 6 7 8 9 10 11 12


Shift Register Yield vs. Margin
y = -4.7220 + 59.235*LOG(x) R^2 = 0.791
shift register yield (%)
power current margin (%)
0
20
40
60
80
100
0 5 10 15 20

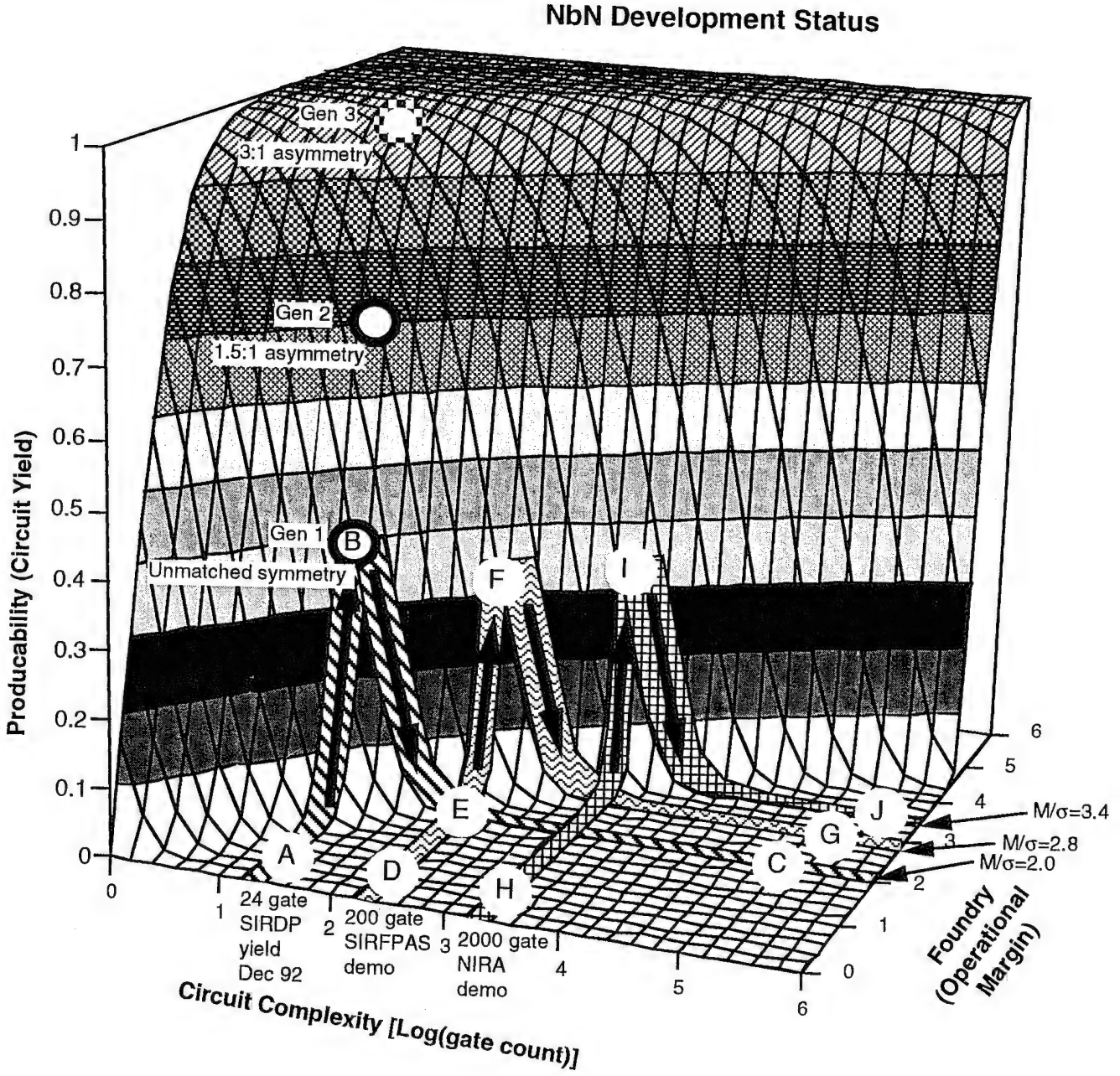
The yield axis in this figure reflects a composite yield including low speed circuit operating margins (M) and variance in chip fabrication uniformity (sigma), primarily Jc, the trilayer critical current. Flux trapping, wafer breakage, and Jc targeting are other factors which contribute to the overall yield.

The initial 24 gate "circuit yield" results implied that the yield metric M/sigma ≈ 2, i.e., that the margins were about twice the spread in the foundry parameters, primarily the Jc, critical current, variance over the circuit tested.

The Jc targeting has been around 20 to 30 %, i.e., one out of 3 to 5 wafers have the required Jc. To achieve a nominal 10% overall yield for circuits of 200 gates, at least 33 % yield of "design and process parameter variations" must be achieved (represented by points "F" and "I" in the figure). These in turn imply required improvement of M/sigma from the Generation 1 of 2.0 to 2.8 to yield 200 gates and 3.4 for 2,000 gates. Moving upward along the M/sigma = 2.8 curve to the 24 gate curve implies a required circuit yield of at least 90 %.

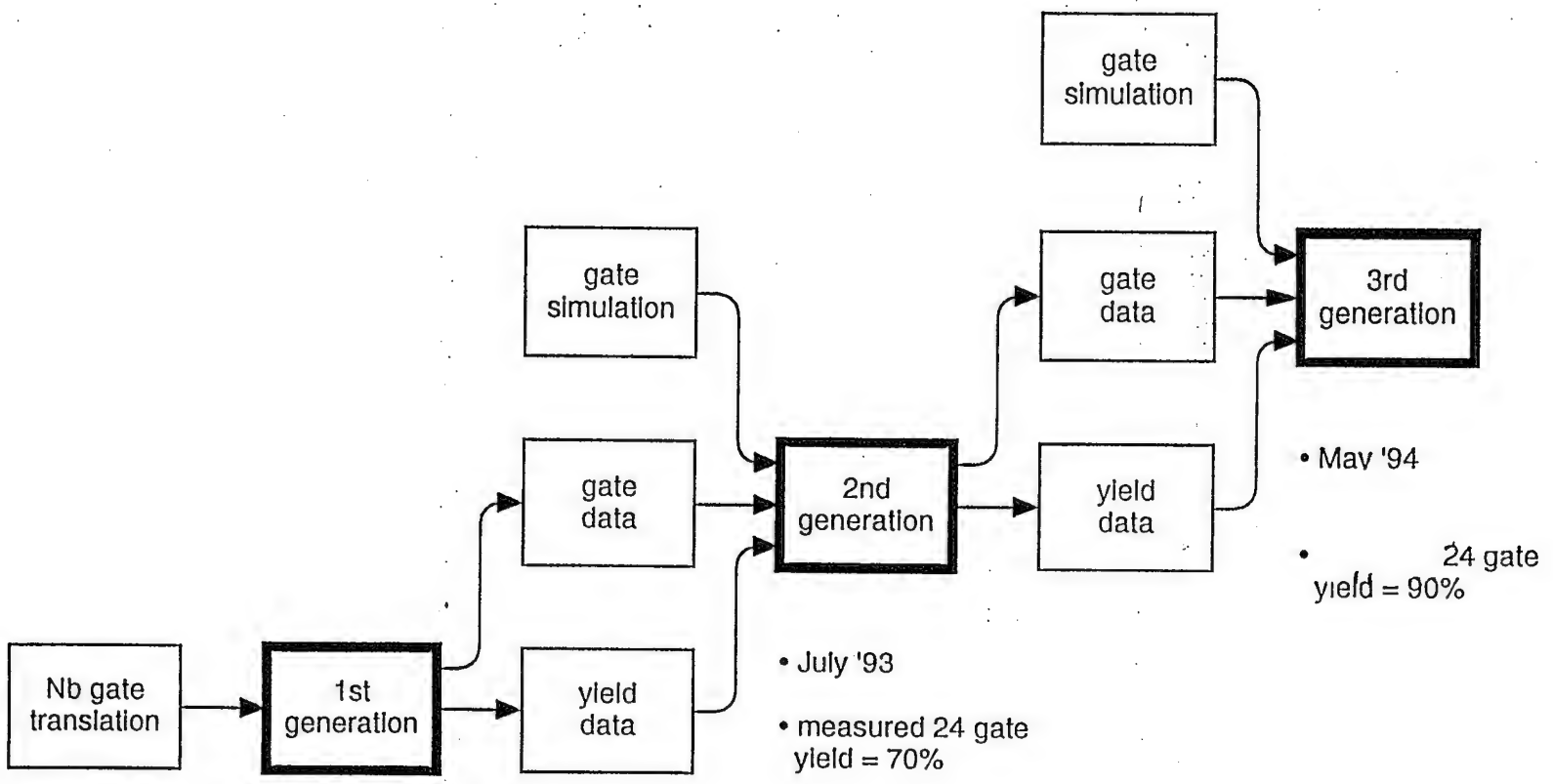
Based on this data, the gate count of 200 for NbN at 10 K was selected as achievable for another project which is to demonstrate and analog to digital converter with a MVTL parallel to serial converter.

The Executive Overview section describes the yield progress for points A, Gen 1, Gen 2, and Gen 3.


NbN Development Status
Gen 3
3:1 asymmetry
Gen 2
1.5:1 asymmetry
Gen 1
Unmatched symmetry
B
F
I
A
D
E
H
C
G
J
Producability (Circuit Yield)
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
1
24 gate SIRDP yield Dec 92
2
200 gate SIRFPAS demo
3
2000 gate NIRA demo
4
5
6
Circuit Complexity [Log(gate count)]
6
5
4
3
2
1
0
Foundry (Operational Margin)
M/σ=3.4
M/σ=2.8
M/σ=2.0

As the foundry process yield improvemented, the NbN circuit yield also dramatically improved going from a single gate in 1992 to hundreds of gates in 1994. The primary improvement evolved around the quantification of the various aspects of the inductances of the modified voltage threshold logic (MVTL) gate structure. Circuit layouts were implemented with specific focus on quantifying the parasitic inductances associated with the circuits and in the reduction of the overall gate circuit inductance.

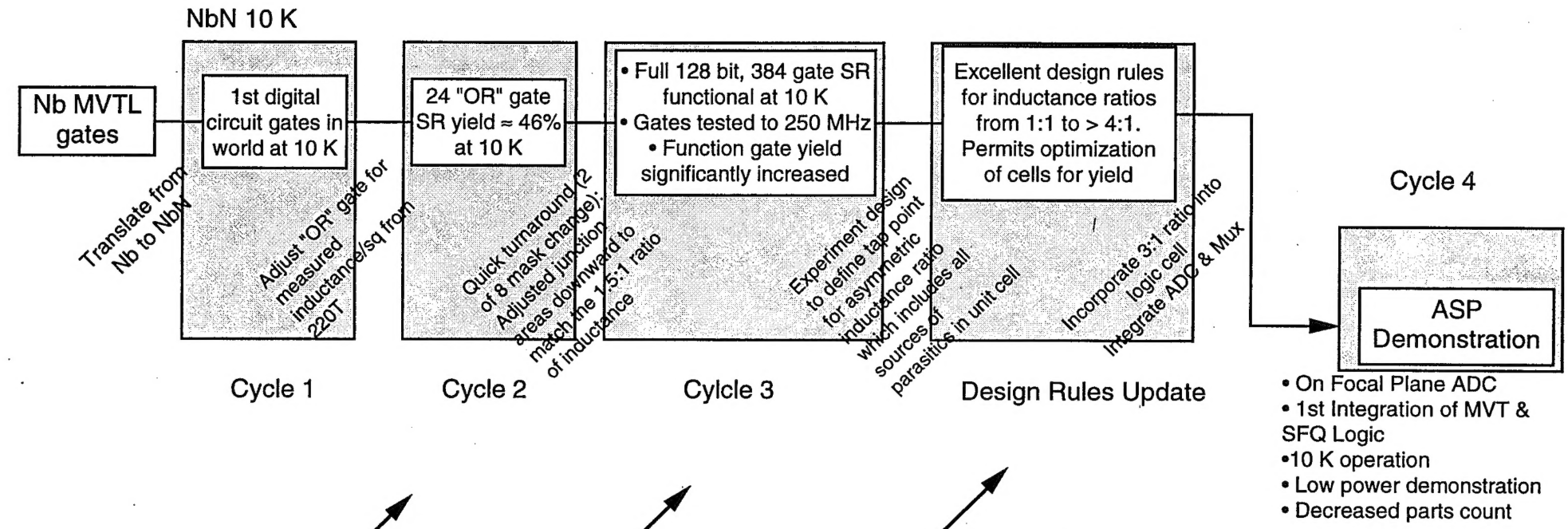
NbN Voltage State Logic Gate Development Enables Progress to 1000 Gate IC's

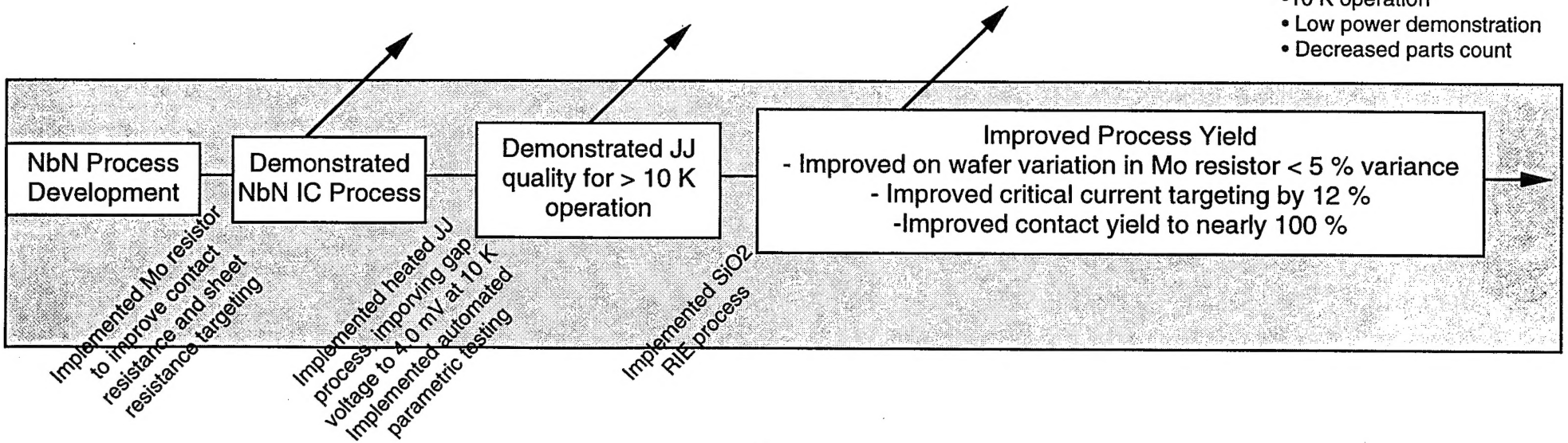


This figure summarizes the steps taken to achieve the dramatic improvement from a single gate in NbN at 10 K at the start of the project to the demonstration of high yield, 400 "OR" gate shift register for 8 to 10 K operation.

Dramatic NbN Circuit Yield Progress

TRW





Technology Maturity Trends:

The tools of the semiconductor industry for thin film processing and integrated circuit manufacturing (lithography, sputtering, ion etching, etc.) are used for superconductive circuit fabrication. Hence little specialized equipment is required for the production of superconductive ICs.

Lead(Pb), the first superconducting IC material was used to develop the basic superconductive digital logic elements and circuit architectures through the '70s. Pb circuits laid the foundation of superconductive ICs but were found to be very unstable. In the early 80s, a reliable process for a Nb JJ was established which was much more controllable and robust relative to the Pb technology. The primary advancement in this technology was made during a five year Japan government/industry thrust between 1983-1989. The maturity rate for Nb was more rapid, using both the semiconductor industry tools and lessons learned from the Pb IC accomplishments.

During the mid 80s, a JJ process for NbN was established. It's pull as a superconductive IC technology came from its ability to operate in the 8-10 K region, a region where SDIO was developing VLWIR sensor systems which operated in this region (a trade between cooling capability and sensor performance). The project summarized in this report evolved from early demonstrations of the NbN technology. The curve shown for NbN is primarily a result of this project supplemented by internal funds. Again, the NbN circuit fabrication and architectures benefited from the accomplishments, procedures and architectures established by the Nb technology, and as Nb and Pb, drew upon the industrial equipment base used by the semiconductor industry. Further progress for NbN is primarily funding limited. As data herein indicates, the uniformity of the NbN process rivals that of Nb.

Note that the curves for the Si IC industry are for off-the-shelf circuits while the superconductor circuits have yet to be inserted into products. Also note that superconductive circuits are tens to hundreds of times faster than the Si circuits, hence superconductive circuit density does not have to match that of Si in order to provide comparable or greater performance. Coupled with the orders of magnitude lower power, superconductive IC technology becomes an enabling technology where W, P, V and power density become issues.

SCE Technology Maturity Trends
History and Projections